

# Mimicking Synaptic Plasticity and Neural Network Using Memtranstors

Jian-Xin Shen, Da-Shan Shang,\* Yi-Sheng Chai, Shou-Guo Wang, Bao-Gen Shen, and Young Sun\*

Artificial synaptic devices that mimic the functions of biological synapses have drawn enormous interest because of their potential in developing brain-inspired computing. Current studies are focusing on memristive devices in which the change of the conductance state is used to emulate synaptic behaviors. Here, a new type of artificial synaptic devices based on the memtranstor is demonstrated, which is a fundamental circuit memelement in addition to the memristor, memcapacitor, and meminductor. The state of transtance (presented by the magnetoelectric voltage) in memtranstors acting as the synaptic weight can be tuned continuously with a large number of nonvolatile levels by engineering the applied voltage pulses. Synaptic behaviors including the long-term potentiation, long-term depression, and spiking-time-dependent plasticity are implemented in memtranstors made of Ni/0.7Pb(Mg<sub>1/3</sub>Nb<sub>2/3</sub>)O<sub>3</sub>-0.3PbTiO<sub>3</sub>/Ni multiferroic heterostructures. Simulations reveal the capability of pattern learning in a memtranstor network. The work elucidates the promise of memtranstors as artificial synaptic devices with low energy consumption.

The progress in information and communication technology requires computers with both time- and energy-efficient data processing. In conventional computers, the rate at which data can be transferred between the central processing unit and the memory units is becoming inefficient because of their traditional von Neumann architecture, that is, the so-called von Neumann bottleneck, caused by physical separation of the computing units and memories.<sup>[1,2]</sup> The human brain appears to provide a natural solution for addressing this bottleneck. As is known, human brain contains  $\approx 10^{10}$  neurons, each connecting to  $\approx 10^4$  other ones on average through synapses, which number

$\approx 10^{15}$  in the human brain. The interconnected neurons can store and process information simultaneously, and their operation is collective and adaptive.<sup>[3]</sup> The special architecture is completely different from the well-established von Neumann one, and can perform massive parallel computing.<sup>[2]</sup> To reproduce similar properties by electronic circuits, many studies have been conducted to develop neuro-morphic computing systems, including those based on software programming and/or based on complementary metal oxide semiconductor devices.<sup>[4–7]</sup> However, some serious challenges exist, such as the energy consumption, complexity of the electric circuit, and the physical size of the computational systems, because complicated algorithms and/or circuits are required just for the functions performed by single neuron or synapse. Therefore,

to mimic effectively the brain operation mode, some nontraditional electronic elements will be required to realize the brain-like information storage and computing.

Memristive devices, i.e., devices that can keep track of the past resistance state through which the element has experienced,<sup>[8,9]</sup> have been widely studied to implement artificial synaptic devices in recent years, because the gradual resistance change of memristive devices driven by external electric signals could be used to reproduce the plasticity of synapses, which is defined as synaptic weight, to represent the strength of the correlation between two neighboring neurons.<sup>[10–25]</sup> Practical implementations of synaptic functions have been realized in various memristive devices with different physical mechanisms, such as phase change,<sup>[10–12]</sup> ferroelectric domains,<sup>[13,14]</sup> magnetoresistance,<sup>[15–17]</sup> and redox-based resistive switching.<sup>[18–26]</sup> In addition to the memristive devices, other candidates and new principles toward artificial synaptic devices are worthy of study.

Recently, we have introduced a fundamental circuit memelement based on the magnetoelectric (ME) coupling effects, i.e., magnetic field control of electric polarization and electric field modulation of magnetization,<sup>[27]</sup> named memtranstor.<sup>[28]</sup> As shown in **Figure 1a**, the fundamental circuit elements are defined by the relationships among four basic circuit variables, i.e., voltage ( $v$ ), current ( $i$ ), charge ( $q$ ), and magnetic flux ( $\varphi$ ). The fourth element defined by the relationship between  $q$  and  $\varphi$  was assigned to the memristor by Chua,<sup>[29]</sup> but remained controversial for many years because of the absence of  $\varphi$  in the memristors.<sup>[30]</sup> It has been realized recently that the true fourth

J.-X. Shen, Dr. D.-S. Shang, Dr. Y.-S. Chai, Prof. B.-G. Shen, Prof. Y. Sun  
Beijing National Laboratory for Condensed Matter Physics  
Institute of Physics

Chinese Academy of Sciences  
Beijing 100190, P. R. China

E-mail: shangdashan@iphy.ac.cn; youngsun@iphy.ac.cn

J.-X. Shen, Prof. Y. Sun

School of Physical Science

University of Chinese Academy of Sciences

Beijing 100190, China

Prof. S.-G. Wang

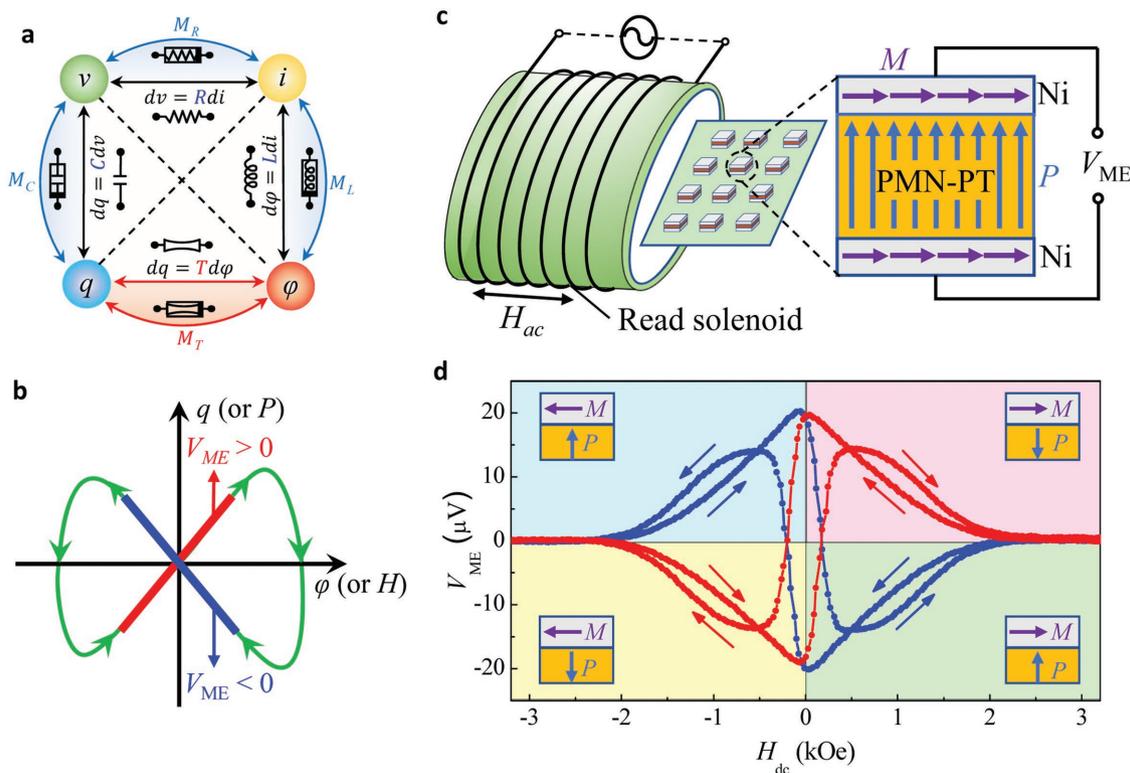
Institute of Advanced Materials

Beijing Normal University

Beijing 100875, China

 The ORCID identification number(s) for the author(s) of this article can be found under <https://doi.org/10.1002/adma.201706717>.

DOI: 10.1002/adma.201706717



**Figure 1.** a) The complete relational diagram of fundamental circuit elements, each defined by a direct relationship between two of four basic variables, voltage ( $v$ ), current ( $i$ ), charge ( $q$ ), and magnetic flux ( $\phi$ ). The diagram consists of four linear elements, namely, resistor ( $R$ ), capacitor ( $C$ ), inductor ( $L$ ), and transtor ( $T$ ), and four nonlinear memelements, namely, memristor ( $M_R$ ), memcapacitor ( $M_C$ ), meminductor ( $M_L$ ), and memtranstor ( $M_T$ ). b) Characteristic behavior of the memtranstor showing a pinched hysteresis loop. The different states of transtance ( $T = dq/d\phi$ ), or equivalently the ME voltage  $V_{ME}$ , are used to store information. c) The structure of the Ni/PMN-PT/Ni memtranstor with in-plane magnetization in the Ni layers and out-of-plane polarization in the PMN-PT layer. An array of memtranstors is placed into a read solenoid that generates a small magnetic field ( $H_{AC}$ ), and the stored information is read out by detecting the induced  $V_{ME}$ . d)  $V_{ME}$  as a function of in-plane DC magnetic field ( $H_{DC}$ ). The polarization is prepooled either upward (blue curve) or downward (red curve). The maximum of  $V_{ME}$  is located around zero field, which is beneficial for practical applications because no bias magnetic field is required.

element defined directly from the  $q$ - $\phi$  relationship can be realized based on the ME coupling effects, termed the transtor.<sup>[28]</sup> Corresponding to the four fundamental elements (resistor, capacitor, inductor, and transtor), there are four memelements (memristor, memcapacitor, meminductor, and memtranstor). The memtranstor is characterized by a butterfly-shaped hysteresis of the  $q$ - $\phi$  relationship, as shown in Figure 1b. Therefore, the quantity called transtance,  $T = dq/d\phi$ , can be switched between positive and negative or high and low states in a non-volatile mode, similar to the switching behavior of resistance,  $R = dv/di$ , in a memristor. The value of transtance is practically proportional to the ME voltage coefficient, which can be measured by inputting a low magnetic field  $H$  to generate an ME voltage ( $V_{ME}$ ) via the ME coupling effect,<sup>[29]</sup> as schematically shown in Figure 1c. Consequently, the states of transtance can be simply represented by the ME voltage  $V_{ME}$  in practical devices.

The memtranstor has a great potential as memory and logic devices because of its nonvolatile switching behaviors and parallel reading mode, as demonstrated recently in a series of experiments.<sup>[31-34]</sup> In particular, the characteristic of nonvolatile multilevel switching, similar to that of memristors, imply a possibility to realize synaptic functions using the memtranstors.

Compared with the memristor, the highly insulating memtranstor has a lower energy consumption because the Joule heating can be effectively reduced.

To explore the potential of memtranstors as artificial synaptic devices for construction of hardware neural networks, in this work we have systemically investigated the multilevel switching behaviors of  $V_{ME}$  in the memtranstors made of Ni/0.7Pb(Mg<sub>1/3</sub>Nb<sub>2/3</sub>)O<sub>3</sub>-0.3PbTiO<sub>3</sub> (PMN-PT)/Ni multiferroic heterostructures that exhibit large ME effects at room temperature. The results clearly demonstrate the emulation of synaptic plasticity using memtranstors. Moreover, the simulations based on experimental data reveal the capability of pattern learning of a neural network made of memtranstors.

The memtranstor used in this work is a typical multiferroic heterostructure consisting of a ferroelectric layer (PMN-PT) and two magnetic layers (Ni). The ME coupling is mainly caused by the interfacial strain between magnetic and ferroelectric layers.<sup>[27]</sup> The top and bottom Ni layers act as not only the magnetic components of the memtranstor but also the electrodes. Figure 1d shows the  $V_{ME}$  of the Ni/PMN-PT/Ni memtranstor as a function of in-plane DC magnetic field ( $H_{DC}$ ) with positive polarization (+ $P$ ) and negative polarization (- $P$ ). Before measuring  $V_{ME}$ , the device is prepooled by applying a positive or a negative

electric field of  $4 \text{ kV cm}^{-1}$  to set the direction of saturation polarization ( $P_s$ ).  $V_{\text{ME}}$  is nearly zero in the high  $H_{\text{DC}}$  region ( $>2 \text{ kOe}$ ) because the magnetization saturation of the Ni layers under which the magnetostriction coefficient is almost zero, resulting in the ME effect of the multiferroic heterostructure being null. When  $P$  is set upward (the red curve),  $V_{\text{ME}}$  increases gradually with  $H_{\text{AC}}$  scanning from 4 kOe to zero and reaches a maximum ( $20 \text{ }\mu\text{V}$ ) near zero field. With  $H_{\text{DC}}$  scanning from positive to negative,  $V_{\text{ME}}$  decreases quickly and the sign changes from positive to negative. After passing a negative peak value ( $-12 \text{ }\mu\text{V}$ ) at  $-0.4 \text{ kOe}$ ,  $V_{\text{ME}}$  is reduced gradually to zero again with increasing  $H_{\text{DC}}$  to 2 kOe. In contrast, when  $P$  is set downward (the black curve), the  $H_{\text{DC}}$  dependence of  $V_{\text{ME}}$  is totally opposite, being negative for positive  $H_{\text{DC}}$  and positive for negative  $H_{\text{DC}}$ . The sign of  $V_{\text{ME}}$  is found to depend on the relative orientation between magnetization and ferroelectric polarization. The ferroelectric polarization of the Ni/PMN-PT/Ni heterostructures can be gradually tuned by fully or partially reversing ferroelectric domains with electric field (see Figure S2, Supporting Information). Thus, when the direction of magnetization remains unchanged, the sign as well as the magnitude of  $V_{\text{ME}}$  can be gradually modulated with pulsed electric fields. The broad hysteresis loop with the maximum value of  $V_{\text{ME}}$  around zero  $H_{\text{DC}}$  promotes practical applications because no DC-bias magnetic field is required for optimizing the performance of the device.

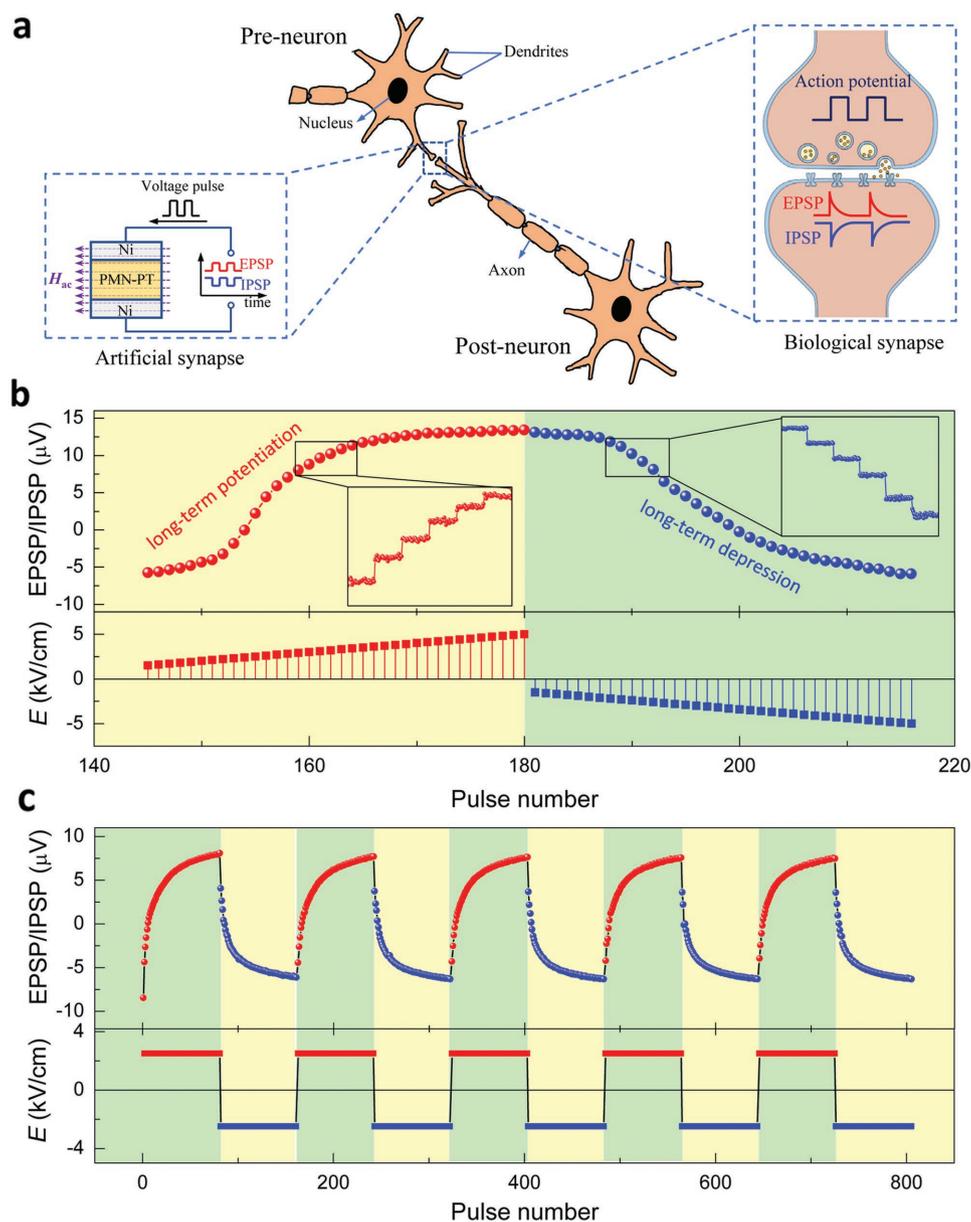
Figure 2b shows the evolution of  $V_{\text{ME}}$  by applying trains of voltage pulses (lower panel) with a fixed time width of 10 ms spaced 100 s apart and increasing amplitude. The  $V_{\text{ME}}$  values are detected at the pulse spacing.  $V_{\text{ME}}$  remains almost unchanged until the amplitude of the applied voltage pulse exceeds a threshold value ( $E = 1.5 \text{ kV cm}^{-1}$ ). Subsequently,  $V_{\text{ME}}$  increases rapidly and then reaches a saturation value ( $13 \text{ }\mu\text{V}$ ), where  $V_{\text{ME}}$  changes little as higher voltage pulses are applied. Reversing the direction of the pulse voltage,  $V_{\text{ME}}$  begins to decrease as the pulse amplitude exceeds a negative threshold value ( $E = -1.5 \text{ kV cm}^{-1}$ ) and then saturates at a low  $V_{\text{ME}}$  state. We also examined the effect of pulse numbers on the  $V_{\text{ME}}$  switching with a constant amplitude. As shown in Figure 2c, a set of 50 voltage pulses with  $E = \pm 2.5 \text{ kV cm}^{-1}$  amplitude, 10 ms width, and 1 s between pulses were applied to the device alternatively. The state of  $V_{\text{ME}}$  is read in the space region. With increasing pulse number,  $V_{\text{ME}}$  increases gradually from  $-8$  to  $8 \text{ }\mu\text{V}$  under the positive pulse stimuli and then decreases to  $-8 \text{ }\mu\text{V}$  under negative pulse stimuli. By both types of voltage pulse stressing, multilevel ME states with different  $V_{\text{ME}}$  values can be obtained. Each ME state shows good stability and can last for a certain period of time (see the insets in Figure 2b and Figure S3 in the Supporting Information). Note that the pulse trains with identical amplitude and the continual switching of  $V_{\text{ME}}$  by varying only pulse numbers, similar to the one used in Figure 2c, are more practical to implement neural network systems in real hardware than the pulse trains with varying amplitudes, like the one used in Figure 2b, because the latter requires the neurons to keep track on the previous activity, which will complicate the design of the peripheral circuits.

The  $V_{\text{ME}}$  switching behavior under electric pulses is analogous to the information transmission characteristics of biological synapses. Figure 2a shows a typical schematic illustration

of a biological synapse. A synapse is a conjunction of two neuron cells, named preneuron and postneuron. Under an external stimulus, spikes or action potentials from the preneuron are transmitted through synapse to the postneuron and generate excitatory postsynaptic potentials (EPSP) or inhibitory postsynaptic potentials (IPSP), together with the synaptic weight updates.<sup>[33]</sup> The information storage and learning of human brains are exactly a consequence of changes in the synaptic weight. Here, the artificial synapse based on memtransistors is achieved by regarding the transconductance value as the synaptic weight and the generated increasing/decreasing  $V_{\text{ME}}$  as the EPSP/IPSP. The applied voltage pulses play the roles of the pre and postsynaptic spikes that act on a memtransistor to modulate the transconductance (i.e., synaptic weight), which is assessed by the detection of  $V_{\text{ME}}$  (i.e., EPSP/IPSP). Therefore, the increasing  $V_{\text{ME}}$  (EPSP) and decreasing  $V_{\text{ME}}$  (IPSP), as shown in Figures 2b,c, indicates the potentiation and depression of the synaptic weight, respectively, that is, synaptic plasticity. In biological systems, the synaptic plasticity can be divided into short-term plasticity and long-term plasticity according to the retention time of the synaptic weight, corresponding to the short-term memory and long-term memory of brain, respectively.<sup>[35–37]</sup> For the Ni/PMN-PT/Ni memtransistor, the obtained transconductance states are quite stable with time. Therefore, the EPSP and IPSP, as shown in Figures 2b,c, can be classed as long-term plasticity, corresponding to the long-term potentiation (LTP) and long-term depression (LTD), respectively.

A well-known theory based on synaptic plasticity is Hebbian learning, which suggests that the synaptic weight is modulated in accordance to neural activities in preneuron and postneuron cells.<sup>[38]</sup> In this form, one of the most important learning rule is spiking-time-dependent plasticity (STDP).<sup>[39]</sup> STDP establishes the synaptic weight adjustment according to the timing of the fired spikes by connected neurons. According to this rule, the synapse potentiates (EPSP or increase of  $V_{\text{ME}}$ ) if presynaptic spikes precede postsynaptic spikes repeatedly, and the synapse depresses (IPSP or decrease of  $V_{\text{ME}}$ ) if postsynaptic spike precedes presynaptic spike repeatedly. The precise pre and post-spike timing window controls the sign and magnitude of synaptic weight modulation.

Based on the plasticity behaviors of the Ni/PMN-PT/Ni memtransistors as a function of pulse amplitude and repetition, STDP is emulated by engineering the pre and postsynaptic superimpositions. As shown in the lower panel of Figure 3a, the prespike is shaped as a pulse train, consisting of the depression (negative voltage) pulses (width = 10 ms) with amplitude increasing from  $V_{\text{pre}} = -1$  to  $-25 \text{ V}$  and potentiation (positive voltage) pulses with amplitude decreasing from 25 to 1 V. The time spacing between two pulses is kept constant (10 ms). The postsynaptic consists of two rectangular pulses (width = 10 ms) with amplitude of  $V_{\text{post}} = 25$  and  $-25 \text{ V}$ . The superimposition between the prespike and the postsynaptic ( $V_{\text{pre}} - V_{\text{post}}$ ) defines the net programming voltage applied on the synapse at each point of time. For example, if a prespike is 20 ms before the postsynaptic ( $\Delta t = 20 \text{ ms}$ ), then the positive part of the postsynaptic will overlap with the second potentiation pulse. The overall potential on the synapse will be above the potentiation threshold ( $V_{\text{th1}}$ ), resulting in an increase in synaptic weight. However, if the postsynaptic is 20 ms before the prespike ( $\Delta t = -20 \text{ ms}$ ), the negative

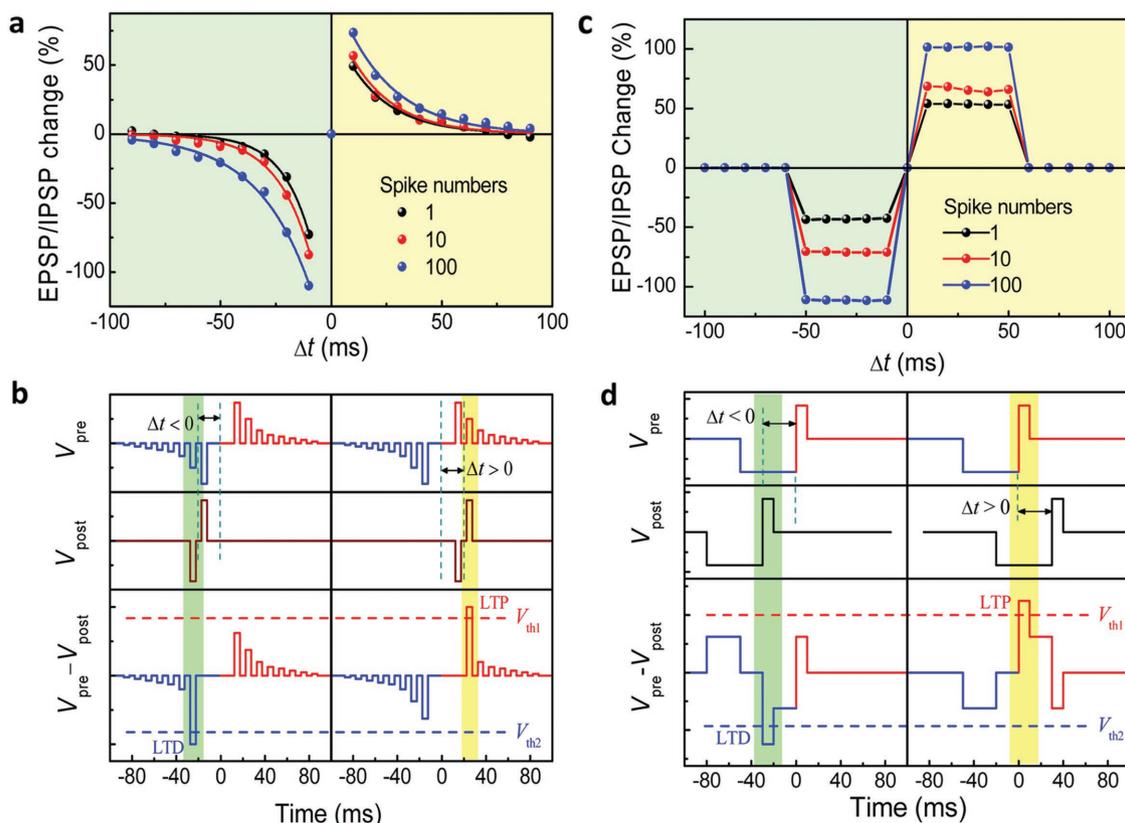


**Figure 2.** a) Schematic illustration of biological neurons and synapses. Right inset: the information transmission between neurons occurs via propagation of action potentials through the axon and release of neurotransmitters, which causes excitatory postsynaptic potentials (EPSP) and inhibitory postsynaptic potentials (IPSP) that would in turn propagate in the postsynaptic axon. Left inset: The memtransistor-based synapse transmits information by applying voltage pulses to change the polarization and subsequently change the ME coupling to produce the  $V_{ME}$  variation. The  $V_{ME}$  plays a role of either EPSP (increase of  $V_{ME}$ ) or IPSP (decrease of  $V_{ME}$ ) in the postsynaptic axon. b) The evolution of the EPSP/IPSP (i.e.,  $V_{ME}$ ) by applying trains of voltage pulses (bottom part) with a fixed time width of 10 ms spaced 100 s apart and increasing amplitude. The  $V_{ME}$  was measured at the pulse spacing. The insets in (b) present enlarged views of each obtained EPSP/IPSP that shows good stability and can last for a certain period of time (100 s for each step). c) The evolution of the EPSP/IPSP (i.e.,  $V_{ME}$ ) by applying voltage pulses with 10 ms width and a constant amplitude of  $E = 2.5 \text{ kV cm}^{-1}$ .

part of the postspike will overlap with the second depression pulse. The overall potential on the synapse will be above the depression threshold ( $V_{th2}$ ), resulting in a decrease in synaptic weight. The change ratio of the synaptic weight can be tuned by changing the action numbers of the identical pre/postspike pairs for each  $\Delta t$ . By repeating the pulse scheme with different  $\Delta t$  in the range from  $-90$  to  $90$  ms, the overall STDP curves are obtained, as shown in the top panel of Figure 3a. The obtained STDP characteristics can be well fitted with exponential

decay functions and conform to the well-known biological synaptic system.<sup>[40]</sup>

In a real biological system, the STDP model should consider the exact value of  $\Delta t$  because an enhanced change in the synaptic weight occurs as  $\Delta t$  is decreased. In the memtransistor-based synapses, the  $V_{ME}$  change can be only dependent on the present  $V_{ME}$  value and the applied pulse numbers according to the experimental data in Figure 2c. Thus, the pulse train with increasing (or decreasing) amplitude is unnecessary for

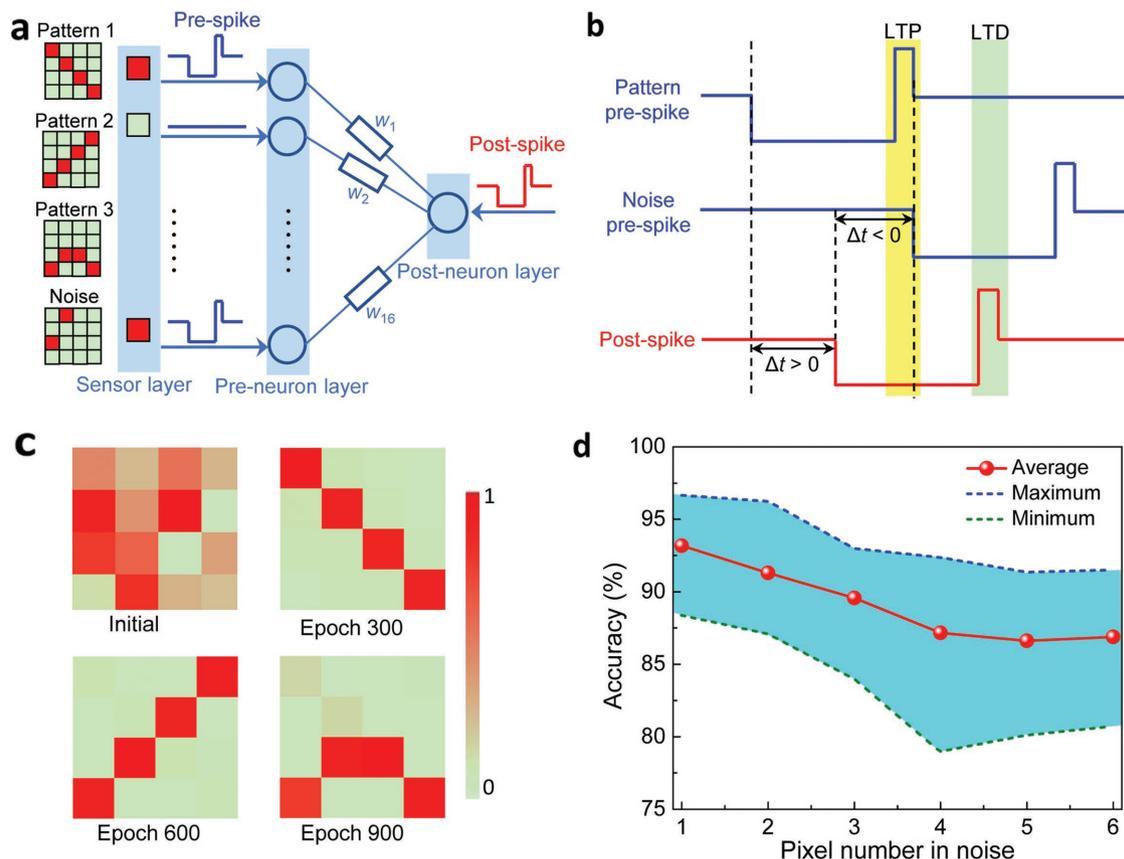


**Figure 3.** a) The experimental data showing the conventional STDP characteristic and b) the corresponding voltage pulse scheme. c) The experimental data following a simplified STDP characteristic and d) the corresponding voltage pulse scheme. The black, red, and blue symbols in (a) and (c) represent the relative change of the EPSP/IPSP versus the relative spiking time ( $\Delta t$ ) obtained by applying 1, 10, and 100 identical pre/postspike pairs for each  $\Delta t$ . In (b) and (d),  $V_{th1}$  and  $V_{th2}$  are the threshold voltage that can induce potentiation and depression of synapses, respectively. By superimposing pre and postspike potentials, the overall potential on the synapse will be above the  $V_{th1}/V_{th2}$ , resulting in the change of the synaptic weight.

the prespike. By using two simplified pulse trains consisting of two rectangular pulses with different width (60 and 10 ms, respectively) and opposite direction, we create a simplified STDP scheme, as shown in Figure 3b. Due to the constant pulse amplitudes of the pre and postspikes, the simplified STDP showed constant potentiation and depression values, that are only determined by the spike numbers, in the region of  $0 < |\Delta t| < 50$  ms for  $\Delta t > 0$  and  $\Delta t < 0$ , respectively. In this case, the timing correlation between the pre and postspikes is converted into the spike numbers applied to the synapses. Compared with the complex pulse trains shown in Figure 3a that generate the biological STDP effect, this simplified STDP learning, which is easily implemented with memtransors, should be more convenient for design of peripheral driving circuitry.

The simplified STDP scheme is employed to simulate the learning ability of an array of memtransors for a predefined pattern with  $4 \times 4$  pixels. The spiking neuron network is modeled by connecting 16 preneurons with one postneuron in parallel through synapses and each preneuron corresponds to one pixel in the pattern, as shown in Figure 4a. The  $4 \times 4$  preneuron layer acts as a retina, emitting spikes in correspondence of a visual pattern. In practice, sensors will sense the pattern and then convert the sensed information into the presynaptic spikes with timings.

A stochastic learning approach is adopted,<sup>[41]</sup> where preneurons are activated alternatively by the predefined pattern and noise at each epoch. Pattern and noise are presented with probability 50% each. The noise consists of two pixels that are randomly distributed. As shown in Figure 4b, we assume that the preneurons corresponding to the pattern pixels will be activated to fire a prespike, labeled as pattern prespike. After a specific delay  $\Delta t$  ( $< 50$  ms), the postneuron fires a postspike to all the preneurons. Because of  $\Delta t < 50$  ms, the postspike will superimpose with the first-part of the prespike to form LTP, which will potentiate the weight of synapses corresponding to the pattern pixels but have no effect on the others. The ending of the pattern prespike will immediately activate the preneurons corresponding to the noise pixels to fire a prespike, labeled as noise prespike. The noise-spike will superimpose the second part of the last postspike to form LTD, which will depress the weight of synapses corresponding to the noise pixels. The above two prespike procedures and one postspike procedure are called one epoch. The synaptic weights are set randomly at the beginning. The neural network is first learned with pattern 1 in Figure 4a to test the learning of a static image, and then patterns 2 and 3 are submitted to demonstrate dynamic learning. The detailed processes of the simulation are described in Figures S1 and S2 and the Supplementary Note in the Supporting Information.



**Figure 4.** a) Schematic illustration of the simulated neuromorphic network. The preneuron layer with 16 neurons is fully connected to one postneuron through 16 memtransistor synapses with synaptic weight  $w_i$ . Three patterns and one random noise image are used for learning. The preneuron layer derives prespikes in response to the presentation of pattern or noise. b) Schematic illustration of the pulse scheme in one epoch where one pattern and then one noise are presented. Long-term potentiation (LTP) and long-term depression (LTD) that occur in the case of pattern and noise presentation, through the simplified STDP learning. c) Evolution of the synaptic weight map during learning. Initial synaptic weights are set randomly. Patterns 1, 2, and 3 with noise are presented in turn for 300 epochs. The weight maps after 300, 600, and 900 epochs show a good adherence to patterns 1, 2, and 3, respectively, thus demonstrating dynamic pattern learning ability. d) The saturation value of the learning accuracy, defined by Equation (1), as a function of the pixel number in noise. The red circles represent the average value from 1000 to 2000 epochs where the accuracy values reach the saturation level. The blue and the green dashed lines indicate the maximum and minimum values obtained in the simulations, respectively, and the other results lie within the shaded cyan area.

Figure 4c shows the simulation results. During the first 300 epochs of learning with pattern 1, the mapping of the synaptic weight shows clearly the same configuration as that of pattern 1, indicating that all the pattern synapses show high  $V_{ME}$ , whereas the background synapses show low  $V_{ME}$ . As the submitted pattern is changed from pattern 1 to pattern 2, the learning of pattern 2 is successful after the second 300 epochs. These findings demonstrate dynamic learning of synaptic weights to the presented pattern in real time by the memtransistor network. Similarly, pattern 3 is learnt during the third phase of 300 epochs. The learning performance can be quantitatively evaluated from the accuracy, which is defined as

$$\text{Accuracy} = \left[ 1 - \sqrt{\frac{\sum_{i=1}^n (V_t(i) - V_i(i))^2}{n}} \right] \times 100\% \quad (1)$$

where  $V_t(i)$  and  $V_i(i)$  are the target and learned  $V_{ME}$ , respectively, at the  $i$ th synapse in a system with a total of  $n$  synapses, and  $V_{ME}$  is normalized to the total plasticity from 0 to 1.

As shown in Figure 4d, the saturation value of the accuracy achieved reaches 91.3% on average (see Figure S3, Supporting Information). In addition, with increasing the pixel numbers to 6 in the noise pattern, the learning accuracy just decreases to 86.9%, indicating a robustness of the memtransistor network against uncontrolled input variability. Note that the noises play a role of background depression in the learning process. Thus, if no noise input, the learning function cannot be realized (see Figure S6, Supporting Information).

The physical process underlying the multilevel transistance (i.e.,  $V_{ME}$ ) switching in the memtransistors can be ascribed to the evolution of the ferroelectric domain configuration in the PMN-PT single crystal. Boyn et al. have systematically studied the ferroelectric domain dynamics and provided a well-established nucleation-limited model to describe the gradual polarization switching in ferroelectric tunnel junctions.<sup>[14]</sup> In essence, this model can also be used to understand the synaptic behaviors in the memtransistors. Distinct from the ferroelectric tunnel junctions, in which the resistance value is regarded as the synaptic weight that is evaluated by monitoring the excitatory postsynaptic

current (EPSC), the synaptic weight of memtranstor-based synapses is represented by the EPSP because voltage signals are directly generated during the reading process. In biology, the EPSP is closer to the real characteristics of nerve cells, such as the membrane potential of the soma than the EPSC.<sup>[42]</sup>

To assess the energy consumption of the memtranstor network, we have calculated the energy for both weight reading and weight change per synapse during the memtranstor working cycle. Because PMN-PT is a good insulator and the leakage current is negligible, the most significant contribution to energy consumption of weight change is the ferroelectric polarization inversion by electric field. The energy density  $J_p$  for ferroelectric polarization inversion can be roughly estimated from  $J_p = 2P_s E_a$ , where  $P_s$  is the maximum intensity of polarization, and  $E_a$  is the applied electric field. According to the saturated polarization ( $\approx 40 \mu\text{C cm}^{-2}$ ) of PMN-PT and the electric field ( $2.75 \text{ kV cm}^{-1}$ ) we used in this study, the energy density for weight change per synapse is calculated to be  $0.22 \text{ J cm}^{-3}$ . Thus, we project an energy cost of  $0.22 \text{ pJ}$  for the weight change of a  $1 \mu\text{m} \times 1 \mu\text{m} \times 1 \mu\text{m}$  memtranstor, which is several orders of magnitude lower than that of the synapses based on conventional CMOS circuit ( $\approx 900 \text{ pJ}$  per stimulation).<sup>[7]</sup> Regarding the weight reading, although the operation mode of the memtranstor is similar to traditional ferroelectric random access memory, the polarization change and rewriting process are not required during the  $V_{\text{ME}}$  reading, that is, the readout is nondestructive. Therefore, the main energy consumption is contributed by the read solenoid, which generates  $H_{\text{ac}}$  for the  $V_{\text{ME}}$  detection. The energy density  $J_m$  of the read solenoid can be estimated by  $J_m = B^2/2\mu$ , where  $B$  is the required magnetic field and  $\mu$  is vacuum permeability. Thus, the magnetic field ( $2 \text{ Oe}$ ) we used for  $V_{\text{ME}}$  reading in this study amounts to  $2 \text{ J cm}^{-3}$ . Note that, for the memtranstor devices with high density arrays, it will be difficult to apply a magnetic field to each memtranstor unit. A feasible approach is to share one magnetic field. Although this approach will enlarge the volume of the magnetic field, that is, the energy consumption, the average energy consumption per memtranstor unit, depending on the storage density of the devices, could be reduced.

In conclusion, we implemented synaptic plasticity in the memtranstors made of Ni/PMN-PT/Ni multiferroic heterostructures that enable the nonvolatile continuous change of the ME coupling voltage. As a proof-of-concept, we demonstrated that by engineering the applied electric pulse which serves as the action potentials, the memtranstance, which is presented by ME coupling voltage and serves as synaptic weight, can perform the LTP, LTD, and STDP of biological synapses. The learning ability of the memtranstor network was demonstrated through a stochastic pattern learning. Combining the advantages of low-power consumption of weight change and nondestructive weight readout, such memtranstor devices have the potential to realize energy-efficient neural networks for building neuromorphic computing systems.

## Experimental Section

**Fabrication of the Devices:** The memtranstors were prepared by depositing Ni on both sides of PMN-PT (110) single crystals by magnetic sputtering to form Ni/PMN-PT/Ni heterostructures, as illustrated in Figure 1b. The size of PMN-PT single crystal is  $5 \times 2 \text{ mm}$ . The

thicknesses of PMN-PT (110) single crystal and the Ni films are  $0.2 \text{ mm}$  and  $1 \mu\text{m}$ , respectively. The ME coupling is mainly caused by the interfacial strain between the magnetic and ferroelectric layers. The top and bottom Ni layers act as not only the magnetic components of the memtranstor but also the electrodes for the output of  $V_{\text{ME}}$ .

**Measurements of the ME Voltage:** A conventional dynamic technique was employed to measure the  $V_{\text{ME}}$  (see Figure S1, Supporting Information). A small AC magnetic field  $H_{\text{AC}}$  at a frequency of  $10 \text{ kHz}$ , generated by an AC source (Keithley 6221) to a solenoid, in the presence of a simultaneous DC bias magnetic field, was applied in plane to the devices. In response, the change in the electric signal ( $V_{\text{AC}} = V_x + iV_y$ ) across the sample resulting from the applied  $H_{\text{AC}}$  was recorded using a lock-in amplifier (Stanford Research SR830) synchronized with the AC current source. To switch or prepole the electric polarization of PMN-PT (110), a sourcemeter (Keithley 6517B) was used to apply voltage pulse across the electrodes. The sample was plugged into an Oxford TeslatronPT superconducting magnet system, which supplies the DC magnetic field. All the measurements were performed at room temperature. To realize automatic measurements, a switcher (Keithley 7001) is used to control the pulse application and the  $V_{\text{ME}}$  reading operations in a program sequence.

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

## Acknowledgements

This work was supported by the National Nature Science Foundation of China (Grant Nos. 11534015, 51671213, 51725104, and 51625101), the National Key Research Program of China (Grant No. 2016YFA0300701), and the Chinese Academy of Sciences (Grant No. XDB07030200).

## Conflict of Interest

The authors declare no conflict of interest.

## Keywords

magnetolectric coupling, memtranstors, multilevel switching, synaptic devices, synaptic plasticity

Received: November 16, 2017

Revised: December 18, 2017

Published online:

- [1] J. Backus, *Commun. ACM* **1978**, *21*, 613.
- [2] G. Indiveri, S. H. Liu, *Proc. IEEE* **2015**, *103*, 1379.
- [3] D. S. Jeong, I. Kim, M. Ziegler, H. Kohlstedt, *RSC Adv.* **2013**, *3*, 3169.
- [4] C. Mead, *Proc. IEEE* **1990**, *78*, 1629.
- [5] M. Mahowald, R. A. Douglas, *Nature* **1991**, *354*, 515.
- [6] J. H. B. Wijekoon, P. Dudek, *Neural Networks* **2008**, *21*, 524.
- [7] G. Indiveri, E. Chicca, R. A. Douglas, *IEEE Trans. Neural Networks* **2006**, *17*, 211.
- [8] L. Chua, *Appl. Phys. A: Mater. Sci. Process.* **2011**, *102*, 765.
- [9] J. J. Yang, D. B. Strukov, D. R. Stewart, *Nat. Nanotechnol.* **2013**, *8*, 13.

- [10] D. Kuzum, R. G. D. Jeyasingh, B. Lee, H. S. P. Wong, *Nano Lett.* **2012**, *12*, 2719.
- [11] T. Tuma, A. Pantazi, M. L. Gallo, A. Sebastian, E. Eleftheriou, *Nat. Nanotechnol.* **2016**, *11*, 693.
- [12] G. W. Burr, R. M. Shelby, S. Sidler, C. Nolfo, J. Jang, I. Boybat, R. S. Shenoy, P. Narayanan, K. Virwani, E. U. Giacometti, B. N. Kurdi, H. Hwang, *IEEE Trans. Electron Devices* **2015**, *62*, 3498.
- [13] Y. Kaneko, Y. Nishitani, M. Ueda, *IEEE Trans. Electron Devices* **2014**, *61*, 2827.
- [14] S. Boyn, J. Grollier, G. Lecerf, B. Xu, N. Locatelli, S. Fusil, S. Girod, C. Carrétéro, K. Garcia, S. Xavier, J. Tomas, L. Bellaiche, M. Bibes, A. Barthélémy, S. Saïghi, V. Garcia, *Nat. Commun.* **2017**, *8*, 14736.
- [15] P. Krzysteczko, J. Münchenberger, M. Schäfers, G. Reiss, A. Thomas, *Adv. Mater.* **2012**, *24*, 762.
- [16] J. Grollier, D. Querlioz, M. D. Stiles, *Proc. IEEE* **2016**, *104*, 2024.
- [17] C. O. Avci, M. Mann, A. J. Tan, P. Gambardella, G. S. D. Beach, *Appl. Phys. Lett.* **2017**, *110*, 203506.
- [18] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, W. Lu, *Nano Lett.* **2010**, *10*, 1297.
- [19] F. Alibart, E. Zamanidoost, D. B. Strukov, *Nat. Commun.* **2013**, *4*, 2072.
- [20] S. Yu, B. Gao, Z. Fang, H. Yu, J. Kang, H. S. P. Wong, *Adv. Mater.* **2013**, *25*, 1774.
- [21] C. S. Yang, D. S. Shang, Y. S. Chai, L. Q. Yang, B. G. Shen, Y. Sun, *Phys. Chem. Chem. Phys.* **2014**, *19*, 4190.
- [22] C. S. Yang, D. S. Shang, N. Liu, G. Shi, X. Shen, R. C. Yu, Y. Q. Li, Y. Sun, *Adv. Mater.* **2017**, *29*, 1700906.
- [23] Z. Wang, S. Joshi, S. E. Savel'ev, H. Jiang, R. Midya, P. Lin, M. Hu, N. Ge, J. P. Strachan, Z. Li, Q. Wu, M. Barnell, G. L. Li, H. L. Xin, R. S. Williams, Q. Xia, J. J. Yang, *Nat. Mater.* **2017**, *16*, 101.
- [24] A. Serb, J. Bill, A. Khiat, R. Berdan, R. Legenstein, T. Prodromakis, *Nat. Commun.* **2016**, *7*, 12611.
- [25] P. Yao, H. Wu, B. Gao, S. B. Eryilmaz, X. Huang, W. Zhang, Q. Zhang, N. Deng, L. Shi, J. S. P. Wong, H. Qian, *Nat. Commun.* **2017**, *8*, 15199.
- [26] Y. Yang, M. Yin, Z. Yu, Z. Wang, T. Zheng, Y. Cai, W. D. Lu, R. Huang, *Adv. Electron. Mater.* **2017**, *3*, 1700032.
- [27] C. Song, B. Cui, F. Li, X. Zhou, F. Pan, *Prog. Mater. Sci.* **2017**, *87*, 33.
- [28] D. S. Shang, Y. S. Chai, Z. X. Cao, J. Lu, Y. Sun, *Chin. Phys. B* **2015**, *25*, 068402.
- [29] L. O. Chua, *IEEE Trans. Circuit Theory* **1971**, *18*, 507.
- [30] N. D. Mathur, *Nature* **2008**, *455*, E13.
- [31] J. X. Shen, J. Z. Cong, Y. S. Chai, D. S. Shang, S. P. Shen, K. Zhai, Y. Tian, Y. Sun, *Phys. Rev. Appl.* **2016**, *6*, 021001.
- [32] J. X. Shen, D. S. Shang, Y. S. Chai, Y. Wang, J. Z. Cong, S. P. Shen, L. Q. Yan, W. H. Wang, Y. Sun, *Phys. Rev. Appl.* **2016**, *6*, 064028.
- [33] J. X. Shen, J. Z. Cong, D. S. Shang, Y. S. Chai, S. P. Shen, K. Zhai, Y. Sun, *Sci. Rep.* **2016**, *6*, 34473.
- [34] P. P. Lu, D. S. Shang, J. X. Shen, Y. S. Chai, C. S. Yang, K. Zhai, J. Z. Cong, S. P. Shen, Y. Sun, *Appl. Phys. Lett.* **2016**, *109*, 252902.
- [35] L. F. Abbott, S. B. Nelson, *Nat. Neurosci.* **2000**, *3*, 1178.
- [36] T. Ohno, T. Hasegawa, T. Tsuruoka, K. Terabe, J. K. Gimzewski, M. Aono, *Nat. Mater.* **2011**, *10*, 591.
- [37] T. Chang, S. H. Jo, W. Lu, *ACS Nano* **2011**, *5*, 7669.
- [38] D. O. Hebb, *The Organization of Behavior*, Wiley and Sons, New York **1949**.
- [39] N. Caporale, Y. Dan, *Annu. Rev. Neurosci.* **2008**, *31*, 25.
- [40] G. Q. Bi, M. M. Poo, *J. Neurol.* **1998**, *18*, 10464.
- [41] S. Ambrogio, N. Ciochini, M. Laudato, V. Milo, A. Pirovano, P. Fantini, D. Ielmini, *Front. Neurosci.* **2016**, *10*, 56.
- [42] J. C. Eccles, *The Physiology of Nerve Cells*, Johns Hopkins Press, Baltimore, MD, USA **1968**.