Graphene-Contacted Ultrashort Channel Monolayer MoS_2 Transistors

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2D semiconductors are promising channel materials for field-effect transistors (FETs) with potentially strong immunity to short-channel effects (SCEs). In this paper, a grain boundary widening technique is developed to fabricate graphene electrodes for contacting monolayer MoS_2. FETs with channel lengths scaling down to ≈4 nm can be realized reliably. These graphene-contacted ultrashort channel MoS_2 FETs exhibit superior performances including the nearly Ohmic contacts and excellent immunity to SCEs. This work provides a facile route toward the fabrication of various 2D material-based devices for ultrascaled electronics.

Conventional silicon-based field-effect transistors (FETs) require their channel thickness being less than one-third of their channel lengths for an effective electrostatic control. Reduction of the channel length into a nanometer regime becomes problematic as short-channel effects (SCEs) arise.[1,2] One typical SCE is known as the drain-induced barrier lowering (DIBL). Even if the channel thickness can be reduced to a few nanometers, the surface would be too rough to avoid severe surface scattering that reduces carrier mobility significantly.[3] Consequently, a potential solution is to find alternative materials such as the recently discovered 2D semiconductor monolayers[4–16] that are naturally ultrathin, ultrasmooth, and free of surface dangling bonds.

Monolayer MoS_2 is a typical 2D semiconductor with a direct band gap of ≈2.2 eV, showing superior electronic and optoelectronic properties.[17–19] Considering its superior immunity to SCEs, it has been predicted that the channel length of a monolayer MoS_2 transistor can be reduced to sub-10 nm.[20–22] Indeed, proof-of-concept devices have been demonstrated recently, including the gated carbon nanotube and partially metallized MoS_2 transistors. The former uses a carbon nanotube to gate monolayer MoS_2 and 3.9/1 nm effective gating length at the OFF/ON state can be realized.[23] No obvious SCEs were observed. The latter uses partially metallized MoS_2 as channels in which a 7.5 nm half-pitch periodic chain of 2H-MoS_2 channel regions is seamlessly connected to 1T′-MoS_2 contact regions.[24] Slight SCEs can be seen. However, both demonstrated device configurations are not standard FETs, i.e., the contact electrodes are away from the channel region.

Standard single-channel short-channel FETs consist of source–drain electrodes directly contacting with the channel. In such devices, fringing effects against the effective gate control originated from the finite thickness of source–drain electrodes could be envisioned as a severe source of SCEs, especially when the thickness of source–drain electrodes is comparable to the channel length.[25] In principle, decreasing the contact metal thickness is a straightforward strategy to weaken the fringing effects. Ideally, using just one-atom-thick metals for contacts will approach the physical limit. Here, we demonstrate

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for the first time the use of one-atom-thick graphene to contact monolayer MoS_2 for the fabrication of FETs with channel lengths as short as ≈4 nm. Graphene contacts are beneficial in terms of not only avoiding the fringing effects but also realizing nearly Ohmic contacts.[26–30] For back-gated monolayer MoS_2 transistors employing with 300 nm SiO_2 as dielectric layers, SCEs emerge when the channel lengths are below ≈16 nm and become severe at a channel length of ≈4 nm. However, for top-gated monolayer MoS_2 transistors employing with few layer hexagonal boron nitride (h-BN) as dielectric layers, devices exhibit significantly improved immunity to SCEs. The 9 nm top-gated devices show no SCEs with a high ON/OFF ratio of 4.5×10^7, low subthreshold swing (SS) of 93 mV·dec^{-1} and a DIBL of 0.425 V·V^{-1}. Top-gated devices of 4 nm show slight SCEs, reflected by the decreased ON/OFF ratio (≈10^6), increased SS (208 mV·dec^{-1}), and increased DIBL (1.23 V·V^{-1}), but still acceptable for a high performance FET.

One technical challenge for the fabrication of graphene-contacted ultrashort channel MoS_2 transistors is how to fabricate graphene gaps with ultrasmooth edges and ultrashort spacing, e.g., a few nanometers. Apparently, standard lithography such as e-beam lithography (EBL) and etching techniques are not able to produce such small gaps, especially for graphene.[25,31] Here, we developed a novel technique to fabricate graphene nanogaps with well-defined gap widths. This technique is lithographic free and uses the 1D grain boundaries (GBs) in monolayer graphene as the active sites for selective hydrogen plasma etching. During etching, GBs are first etched out then widened into nanogaps, as illustrated in **Figure 1**a. Note that, by using appropriate etching temperature and plasma doses, this hydrogen plasma etching does not etch the perfect lattice within the graphene basal plane.[32–34] This lateral etching rate, usually a few nm•min^{-1}, is very stable at fixed etching temperatures and plasma doses. Thus, we could solely use the etching time T to tune the gap widths W of graphene in a precisely controlled manner. Figure 1b shows the W–T relationship for two graphene samples on 300 nm SiO_2/Si(n++) substrates (#1 with GBs and #2 with an already formed 50 nm gaps fabricated by EBL and oxygen plasma etching). Hydrogen plasma etching was performed at a pressure of ≈0.29 Torr, a radiofrequency reflection power of ≈25 W, and a substrate temperature of ≈250 °C. Both samples show very consistent etching rate k ≈3 nm min^{-1}. Please also see the Supporting Information for more details. Figure 1c/d shows a typical atomic force microscopy (AFM)/scanning electron microscopy (SEM) image of a nanogap in graphene after GB etching for 2.5 min using the above-mentioned etching condition. The assumed W = 7.5 nm and the measured W ≈8 nm match quite well.

Using the etched graphene nanogaps as electrodes, we thus are able to fabricate ultrashort channel MoS_2 FETs on 300 nm SiO_2/Si(n++) substrates. The step-by-step fabrication process is illustrated in **Figure 2**a. Mechanically exfoliated monolayer MoS_2 was first transferred over the graphene nanogap; then, EBL and oxygen plasma etching processes were performed to define the device geometry. In the following step, metal leads were wired out for measurements. These back-gated devices can be upgraded into dual-gated configurations by further transferring ultrathin h-BN sheets to cover the channel region and wiring out top-gated electrodes. The dual-gated/back-gated device structure is illustrated in Figure 2b/c. Please also see the Supporting Information for more details on device fabrication.

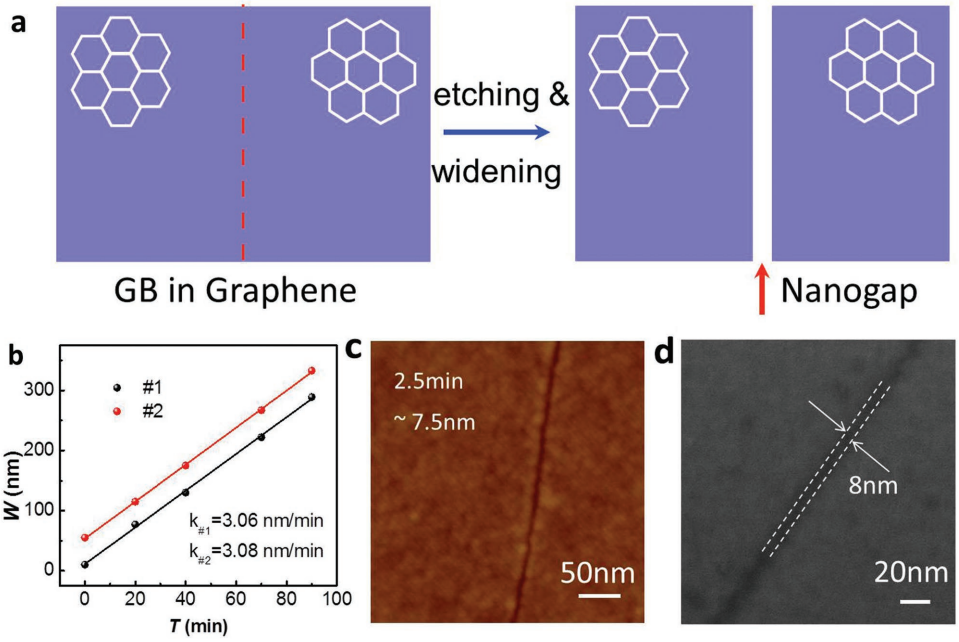

Figure 1. Characterization of etched gaps in graphene from grain boundaries by H_2 plasma. a) Schematic of the H_2 plasma etching effect on a graphene GB. b) Time-dependent etched gap widths of two graphene samples (samples #1 with grain boundaries and samples #2 with an already formed 50 nm gaps fabricated by EBL and oxygen plasma etching). $k_{\#1}$ and $k_{\#2}$, extracted as the slopes of the fitting lines, are the H_2 plasma etching rates in graphene samples #1 and #2, respectively. Etching condition: pressure ≈0.29 Torr, RF power ≈25 W, and substrate temperature of ≈250 °C. c) Typical AFM image and d) SEM image of a nanogap in graphene after GB etching for 2.5 min using this etching condition.

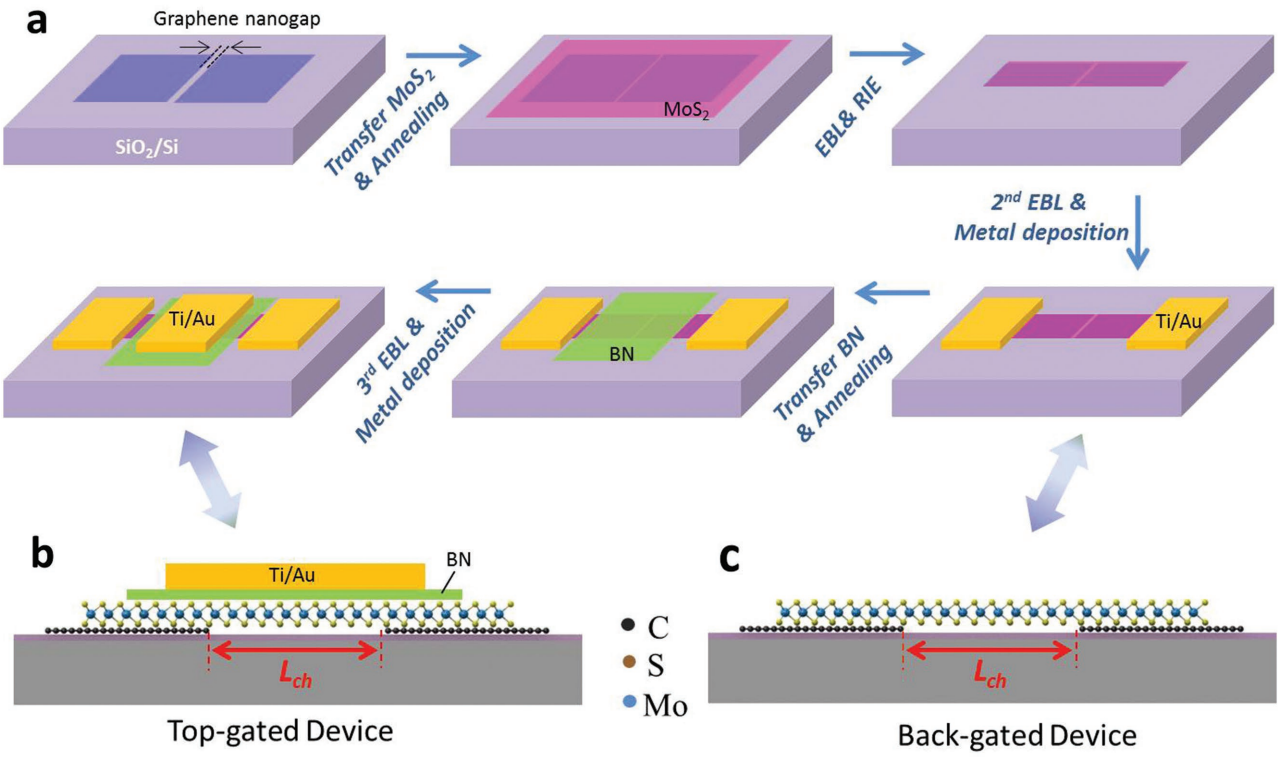

Figure 2. Device fabrications. a) Schematic illustration of the fabrication process of graphene-contacted ultrashort channel MoS_2 transistors. b,c) Atomic sectional drawing of a device in top-gated/back-gated geometry.

The quality of MoS_2/graphene interface can be reflected by optical characterization such as Raman and photoluminescence (PL) spectra. Figure S6 in the Supporting Information shows the Raman and PL spectra of the MoS_2/graphene sample. As a comparison, bare monolayer MoS_2 gives two typical Raman peaks at ≈385.3 cm^{-1} (E_{2g} mode) and 404.9 cm^{-1} (A_{1g} mode).[35] While in MoS_2/graphene, 1.4 cm^{-1} increment of the E_{2g}–A_{1g} peak spacing was observed and attributed to the interlayer coupling between two layers. This larger peak spacing and quenched PL intensity also suggest good contact in graphene/MoS_2 heterostructure.[36,37]

First, we investigated the performance of the back-gated ultrashort channel FETs (an illustrated device is shown in **Figure 3**a. The output characteristics of two typical devices with channel lengths of ≈8 and ≈3.8 nm are shown in Figure 3b,d, respectively. The linearity of *I*–*V* curves suggests the superiority of graphene contacts in MoS_2 transistors.[30,38] The current density at V_{DS} = 100 mV and V_{BG} = 60 V of the 8/3.8 nm device is 8.1/9 μA $μm^{-1}$. This small difference suggests that the contact resistances are dominant in the total device resistances. The transfer characteristics of the two devices are shown in Figure 3c,e, exhibiting clear n-type transistor behavior. For the 8 nm device, the ON/OFF ratio is ≈1.5×10^6, which is similar to that of long-channel devices reported previously.[39–42] The ON/OFF ratio also changes very little with increased V_{DS}, indicating a low DIBL. For the 3.8 nm device, the ON/OFF ratio is ≈5×10^5, suggesting the emergence of obvious SCEs. Corresponding gate leakage currents are also displayed in Figure S7 in the Supporting Information.

We also tested the current load ability of such short-channel FETs. Figure 3f shows a typical *I*–*V* curve of a 10 nm device. The maximum current density can approach to 540 μA $μm^{-1}$ at a bias voltage of 3.5 V before device's break down. This current density is at least two orders of magnitude higher than that of long-channel monolayer MoS_2 transistors with metal contacts under similar bias conditions.[43] Please also see Figure S8 in the Supporting Information for more details.

In ultrashort channel devices, the contact resistances are prominent. The total resistance R of a transistor can be described as $R = R_{ch} + 2R_c$, where R_{ch} is the channel resistance and $2R_c$ is the contact resistance. $2R_c$ consists of the graphene/MoS_2 contacts ($2R_{Gr\text{-}MoS2}$), graphene electrodes ($2R_{Gr}$), and metal/graphene contacts ($2R_{Metal\text{-}Gr}$). In order to obtain the intrinsic field-effect mobility (μ) of the devices, we must exclude these contact resistances by the transfer length method (TLM).[41,42] Thus,

$$\mu = \frac{dI_{DS}}{dV_{BG}} \cdot \frac{L_{ch}}{W} \cdot \frac{1}{V_{DS}} \cdot \frac{R}{R-2R_c} \cdot \frac{1}{C_i} \quad (1)$$

where L_{ch} is the channel length, W is the channel width, and $C_i = 1.15 \times 10^{-4}$ F·m^{-2} is the capacitance per unit area of the 300 nm thick SiO_2 gate dielectric.

Figure 4a shows a series of devices with different channel lengths (L_{ch} = 0.4, 0.6, 0.8, 1.0, and 1.2 μm) for TLM measurements. Note that the gaped graphene electrodes in these devices were fabricated by standard lithographic and etching techniques since the gaps are wide enough. The detailed design

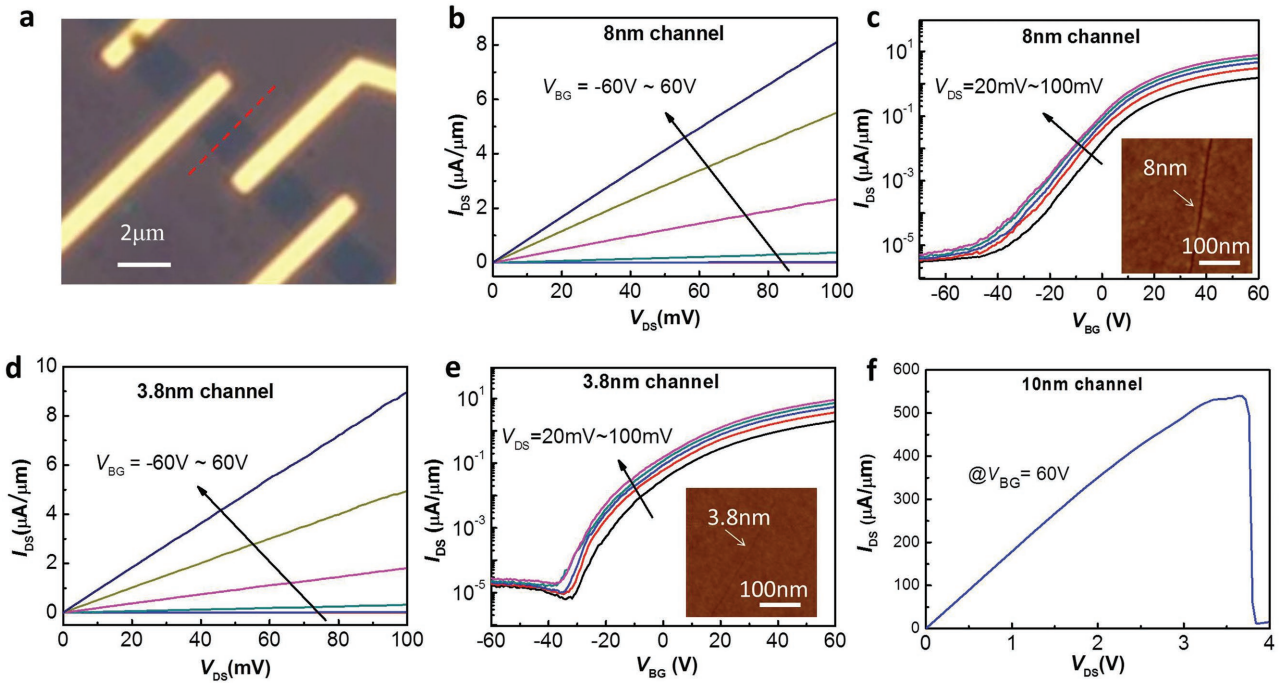

Figure 3. Electronic characterization of graphene-contacted ultrashort channel back-gated monolayer MoS_2. a) OM image of a typical ultrashort channel back-gated monolayer MoS_2. b) and d) Typical output curves of 8nm and 3.8 nm MoS_2 FETs at various back-gated voltages, respectively. c) and e) Semi-log plot of transfer characteristics of 8nm and 3.8 nm MoS_2 FETs at various bias voltages, respectively. Insets of c and e are the AFM images of graphene with widened grain boundaries ~ 8nm- and 3.8 nm-wide, respectively. f) The current load ability test curve performed on a 10 nm channel device. The current density rushed into 540 μA μm^{-1} at V_{DS} = 3.5 V till the device's broke down.

and fabrication process can be seen in Figure S9 in the Supporting Information. Figure 4b shows the R–L_{ch} relationships at four typical V_{BG}. For long-channel MoS_2 transistors, devices work in the diffusive regime, in which R can be written as $R = \rho L_{ch} + 2R_c$, where ρ is the 2D channel sheet resistance. Hence, $2R_c$ and ρ can be extracted as the intercept and slope of the linear fit to R–L_{ch} curves. The extracted $2R_c$ and ρ are plotted in Figure 4c. We can see that both $2R_c$ and ρ decrease obviously at higher carrier concentrations. At V_{BG} = 60 V, R_c is 4.8 kΩ·μm, with $R_{Gr} + R_{Metal\text{-}Gr}$ about to ≈1 kΩ·μm. Therefore, we obtain $R_{Gr\text{-}MoS2}$ of ≈3.8 kΩ·μm, which agrees well with the previously reported results (Table S1, Supporting Information).[38,44,45] By excluding the $2R_c$, we plotted the intrinsic transfer curve of the 3.8 nm device at V_{DS} = 100 mV in linear coordinate (Figure 4d, black dots). The calculated intrinsic field effect mobility is ≈26.7 $cm^2\ V^{-1}\ s^{-1}$ at V_{BG} = 60 V, being close to the previous reported mobilities of long-channel monolayer MoS_2 devices,[39,40] and also suggesting such ultrashort channel devices still work in the diffusive regime.

To further investigate the channel length scaling behavior of back-gated MoS_2 FETs, we then measured many devices with different L_{ch} (Figure S10, Supporting Information). The corresponding ON/OFF ratios, mobilities (μ), SS, and DIBL of these devices are extracted and listed in Figure 4e. We can see that both μ and ON/OFF ratios decrease with L_{ch}, but not in a serious manner. As L_{ch} shrinks down to 3.8 nm, the OFF current density remained at a value lower than 15 pA μm^{-1}, which could satisfy the International Technology Roadmap for Semiconductors (ITRS) low-operating-power 2024 requirements.[46]

Despite the ON/OFF ratios, devices' SS and DIBL are another two important characteristics subjected to SCEs. At L_{ch} < 16 nm, both SS and DIBL show obvious increase, suggesting that SCEs start to emerge. The emergence of SCEs is due to the fact that a device's L_{ch} is comparable to its characteristic length (λ). We thus calculated λ for these back-gated devices by

$$\lambda = \sqrt{\frac{\varepsilon_s}{\varepsilon_{ox}} t_s t_{ox}} \tag{2}$$

where ε_s, ε_{ox}, t_s, and t_{ox} are semiconductor dielectric constant, gate oxide dielectric constant, semiconductor thickness, and gate oxide thickness, respectively. In the present case, ε_s = 3.3, ε_{ox} = 3.9, t_s = 0.6 nm, and t_{ox} = 300 nm, thus $\lambda \approx$ 12.3 nm, which match with the above results.

One effectiveway to enhance the gating efficiency and meanwhile reduce λ is to employ the thinner gate dielectric layers. We thus fabricated dual-gated devices with <5 nm thick h-BN ($\varepsilon_{ox} \approx 4$) as top-gated dielectrics. An illustrated device is shown in **Figure 5**a. With this top-gated configurations, $\lambda \approx$ 1.8 nm, which is significantly reduced compared with that in back-gated configurations. Figure 5b–d shows the characteristics of two typical devices with L_{ch} = 9 nm (h-BN thickness: ≈4 nm) and L_{ch} = 4 nm (h-BN thickness: ≈2.5 nm); and Figure 5e shows statistic data from many devices with different L_{ch}. We can see that, at L_{ch} > 9 nm, devices are free of SCEs with ON/OFF ratios >4.5×10^7, OFF current density <0.3 pA μm^{-1}, μ > 30 $cm^2\ V^{-1}\ s^{-1}$, SS < 93 mV·dec^{-1}, and DIBL < 0.425 V·V^{-1}. At L_{ch} = 4 nm, which is close to the characteristic length, the device's ON/OFF

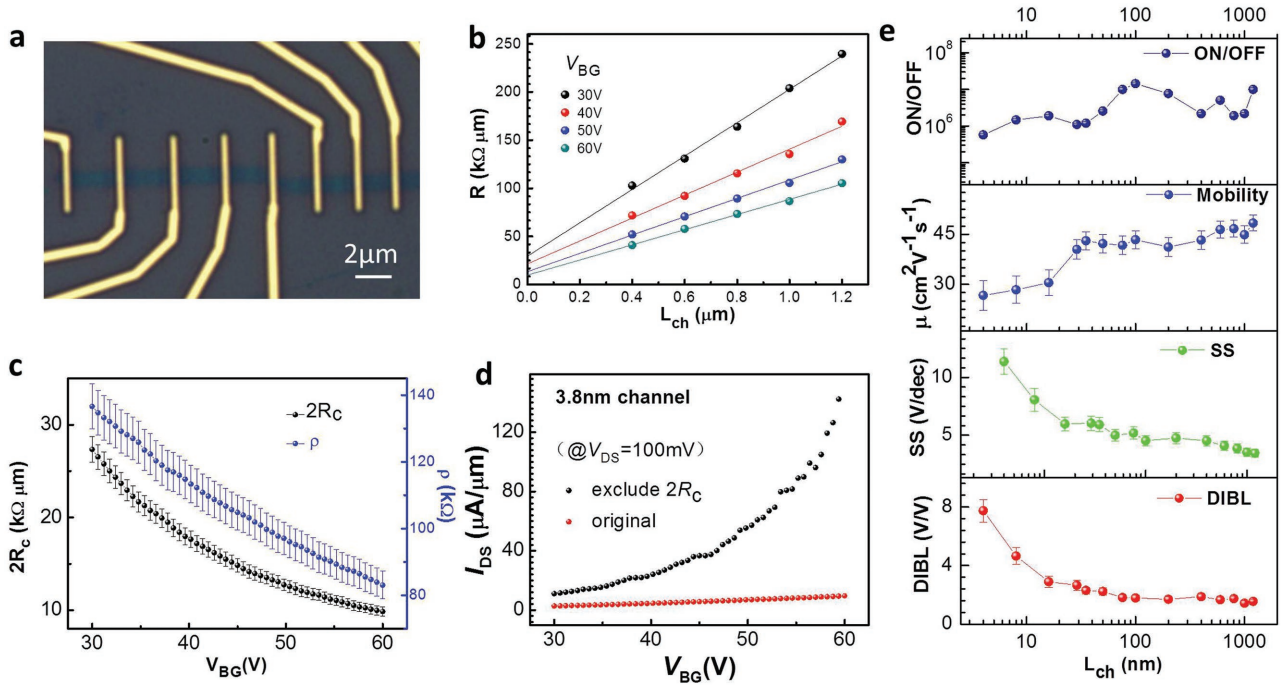

Figure 4. Contact resistance deducting and channel length scaling behavior of back-gated MoS_2 transistors. a) Optical image of the back-gated MoS_2 transistors in TLM geometry. b) Total resistance R versus channel length L_{ch} at various back-gated voltages. Solid lines are the linear fits. c) Contact resistance $2R_c$ and MoS_2 sheet resistance ρ extracted from the linear fits at multiple back-gated voltages. d) Original (red dots) and corrected (black dots) transfer curves (@V_{DS} = 100 mV) of the 3.8 nm device at the range of 30 V < V_{BG} < 60 V. e) Channel length-dependent ON/OFF ratio, intrinsic field-effect mobilities, subthreshold swing, and drain-induced barrier lowering of back-gated MoS_2 transistors.

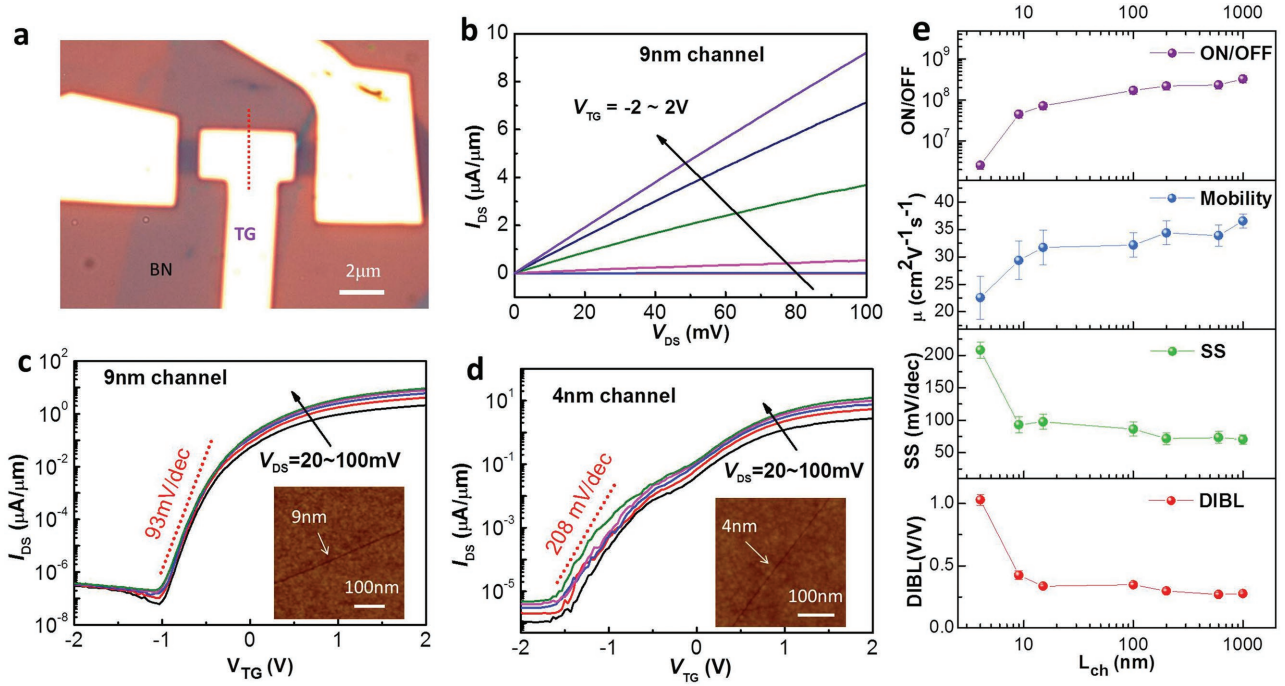

Figure 5. Electronic characterization of graphene-contacted ultrashort channel top-gated MoS_2 devices and their channel length scaling behavior. a) OM image of a typical ultrashort channel top-gated MoS_2 transistor. Red dashed line marks the location of channel. b) Typical output curves of a 9 nm channel top-gated MoS_2 transistor at various top-gated voltages. c) and d) Semi-log plots of transfer characteristics of the 9nm and 4 nm top-gated MoS_2 transistors at various bias voltages, respectively. Insets of c and d show the AFM image of graphene with widened grain boundaries ≈9nm- and 4 nm-wide. e) Channel length-dependent ON/OFF ratio, intrinsic field-effect mobilities, subthreshold swing, and drain-induced barrier lowering of top-gated MoS_2 transistors.

ratio, OFF current density, SS, and DIBL degrade to $\approx 2.6 \times 10^6$, 5 pA μm^{-1}, 208 $mV \cdot dec^{-1}$, and 1.03 $V \cdot V^{-1}$, respectively, indicating the presence of slight SCEs but still being acceptable for high performance FETs. Please see more data and analysis in the Supporting Information.

In conclusion, we developed a novel method to fabricate ultrashort channel monolayer MoS_2 FETs contacted by monolayer graphene. The electrical performance of these FETs with channel lengths >4 nm was systematically investigated. We found that devices with channel length above 9 nm show extraordinary immunity to SCEs. For devices with channel lengths below 9 nm, SCEs appear but still being acceptable, as illustrated by a 4 nm ultrashort channel device. This work provides a facile route toward the fabrication of various 2D material-based devices for ultrascaled electronics.

Experimental Section

Graphene Nanogaps Fabrication: Monolayer graphene flakes were mechanically exfoliated by Scotch tape from a bulk graphite (HOPG, grade ZYA, from Materials Quartz, Inc.) onto a 300 nm SiO_2 substrate. The as-exfoliated graphene samples were annealed in gas mixture H_2/Ar (10 sccm/150 sccm) for 60 min at 450 °C to remove tape residuals and then etched by H_2 plasma in the R-PECVD system at a substrate temperature ≈250 °C, and the H_2 pressure and plasma power were 0.29 Torr and 25 W, respectively. The widths of the etched graphene nanogaps were tuned by etching time. The as-fabricated graphene nanogaps were characterized by AFM (MultiMode IIId, Veeco Instruments) using a tapping mode at room temperature in an ambient atmosphere and SEM (Raith-eline) at an acceleration voltage of ≈3kV and vacuum ≈10^{-7} mbar.

Device Fabrication: MoS_2/graphene heterostuctures were prepared by transferring mechanically exfoliated MoS_2 flakes onto nanogapped graphene through our homemade transfer system. As transferred MoS_2/nanogapped-graphene heterostuctures were spin coated with a polymethylmethacrylate (PMMA) photoresist followed by EBL (Raith-eline) and O_2 plasma etching to define the channel. Then, metal electrode leads were patterned by the second EBL and metal deposition (3 nm Ti and 40 nm Au) in electron beam evaporation. BN flakes used as gate dielectric layers in top-gated devices were mechanically exfoliated from bulk h-BN provided by Prof. Kenji Watanabe and Prof. Takashi Taniguchi in National Institute of Material Sciences (NIMS) in Japan. We transferred ultrathin BN flakes to cover the channel regions of back-gated devices through our homemade transfer system, which results in dual-gated devices.

Device Characterization: The Raman and PL spectra were carried out on a Horiba Jobin Yvon LabRAM HR-Evolution Raman microscope (Paris, France) with an excitation laser wavelength of 532 nm, a laser power of 10 mW, and a laser spot size of ≈1 μm at room temperature. The electrical characterization was carried out in a close-cycle cryogenic probe station with a base pressure of 10^{-7} Torr at room temperature.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

G.Z. conceived and designed the research. L.X. fabricated the devices and performed the measurements. M.L. provided assistance with the transfer technique. S.P.W. provided assistance for top-gated devices fabricating. J.T. provided exfoliated large-area and ultrathin hexagonal boron nitride samples for the dielectric layers in the top-gated devices. L.X., D.S., and G.Z. prepared the manuscript. All authors discussed the results and commented on the manuscript. G.Z. would like to thank Prof. Kenji Watanabe and Prof. Takashi Taniguchi in the National Institute of Material Sciences (NIMS) in Japan to provide us h-BN flakes. G.Z. acknowledges supports from the National Key R&D program under Grant No. 2016YFA0300904, the National Basic Research Program of China (973 Program, Grant No. 2013CB934500), the National Science Foundation of China (NSFC, Grant No. 61325021), the Key Research Program of Frontier Sciences, CAS (Grant No. QYZDB-SSW-SLH004), and the Strategic Priority Research Program (B), CAS (Grant No. XDB07010100). D.S. acknowledges supports from the National Science Foundation of China (NSFC, Grant No. 51572289). R.Y. acknowledges supports from the National Basic Research Program of China (973 Program, Grant No. 2013CBA01602) and the National Science Foundation of China (NSFC, Grant No. 11574361). G.X. acknowledges supports from the National Key Laboratory of Science and Technology on Space Microwave (No.6142411010101).

Conflict of Interest

The authors declare no conflict of interest.

Keywords

graphene contacts, MoS_2, short-channel effects, ultrashort channels

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