nature COMMUNICATIONS

ARTICLE

Received 9 Jul 2013 | Accepted 11 Oct 2013 | Published 8 Nov 2013

DOI: 10.1038/ncomms3764

In situ electron holography study of charge distribution in high-κ charge-trapping memory

Y. Yao[1,*], C. Li[1,*], Z.L. Huo[2], M. Liu[2], C.X. Zhu[2], C.Z. Gu[1], X.F. Duan[1], Y.G. Wang[1], L. Gu[1] & R.C. Yu[1]

Charge-trapping memory with high-κ insulator films is a candidate for future memory devices. Many efforts with different indirect methods have been made to confirm the trapping position of the charges, but the reported results in the literatures are contrary, from the bottom to the top of the trapping layers. Here we characterize the local charge distribution in the high-κ dielectric stacks under different bias with *in situ* electron holography. The retrieved phase change induced by external bias strength is visualized with high spatial resolution and the negative charges aggregated on the interface between Al_2O_3 block layer and HfO_2 trapping layer are confirmed. Moreover, the positive charges are discovered near the interface between HfO_2 and SiO_2 films, which may have an impact on the performance of the charge-trapping memory but were neglected in previous models and theory.

[1] Beijing National Laboratory of Condensed Matter Physics, Institute of Physics, Chinese Academy of Sciences, Beijing 100190, China. [2] Laboratory of Nano-Fabrication and Novel Devices Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China. * These authors contribute equally to this work. Correspondence and requests for materials should be addressed to Y.Y. (email: yaoyuan@iphy.ac.cn).

Charge-trapping memory (CTM) with high-κ dielectric substituting floating gate as the charge capture layer is a candidate for next-generation storage devices as it radically improves the retention force, weakens the coupling effect and the charge leakage. The elusive spatial charge distribution in the CTM has an important role influencing the programme/erase speed and the retention force. Therefore, it is critical to map the charge distribution in the dielectric layers to clear the trapping mechanism of CTM and improve the design and fabrication process to ensure the performance of the future memory devices. I–V and C–V measurements are the usual characterization tools to deduce the charge distribution along vertical direction of the charges with the appropriate models. However, these methods concerning models only depict the effective charge distribution with a poor spatial resolution and moreover, these indirect electrical investigations can be disturbed so easily by the measurement environment or parameters that controversial results were reported in the literatures. You *et al.*[1] thought that the electrons were bulk trapped in the HfO_2 trap layer but interface trapped in the Si_3N_4 trap layer. Zhu *et al.*[2] indicated that the trapped charges located in both interface and bulk in the HfO_2 layer. Bu and White[3] found that the charges concentrated on the interface between the block and trap layer, whereas Zahid *et al.*[4] reported that electrons aggregated in the interface between the metal gate and block Al_2O_3 layer and those electrons could vary the threshold voltage, which was confirmed by Rao *et al.*[5] and Padovani *et al.*[6] Sharma *et al.*[7] showed that the holes generated in the SiO_xN_y trap layer might cause the profiled electron centroid moving towards the HfO_2 block layer. Ko *et al.*[8] pointed that oxygen interstitials or Hf vacancies, beside the oxygen vacancies, may have the important roles as the charged point defects in charge-trapping process. Ramanathan *et al.*[9] noted that the C–V curve could not perfectly reflect the charge-trapping phenomena because of the complexity of test environment. Recently, several types of scanning probe microscopy (SPM), such as electrostatic force microscope[10], Kelvin force microscope[11], scanning capacitance microscope[12] and conductive atomic force microscope[13], have been used to profile the charge distribution in CTM with tens of nanometre resolution. SPM can track the lateral charge map and diffusion process but the working mode and the limited spatial resolution impede it to distinguish the vertical location of the trapped charges, which have an impact significantly on the performance of the device. Therefore, a direct observation is urgently needed to clarify the charge location in CTM.

Electron holography is a powerful means to image the electrostatic potential distribution because the charges in the sample can alter the phase of the penetrated electron wave and such phase disturbance can be retrieved from the electron interference patterns. Electron holography in transmission electron microscope (TEM) has been employed to map the depletion layer in *p–n* junction[14], the interfacial polarization field in the superlattices[15], two-dimensional electron gas and two-dimensional hole gas in the high electron mobility transistor device[16] and the charge distribution in nanomaterials[17]. Combined with *in situ* techniques, the bias-induced potential variations in *p–n* junction[18] and metal oxide semiconductor (MOS) transistor[19] were imaged. It should be noted that electron holography in TEM possesses the merit to snapshot the potential image with high spatial resolution, which is extremely important for the characterization of nanometre materials and devices.

In this paper, *in situ* electron holography in TEM has been adapted to map the vertical and lateral charge distribution within the CTM simultaneously. Benefited by the high-resolution electron holography, the charge-trapping process traced under different gate biases indicates unambiguously that the electrons penetrate through the HfO_2 layer and aggregate beneath the interface between HfO_2 and $Al2O_3$ films.

Result

Structure and *in situ* I–V characterization. The schematic diagrams of the *in situ* measurements and the hologram acquirements are shown in Fig. 1a,b, respectively. Conventionally, the reference wave in electron holography is the beam passing through the vacuum. However, in principle every wave with known or invariant phase distribution, for example, the electron beam penetrating the Al gate layer here, is also available to preserve the relative phase difference feature between the insulator layers and the Si substrate[20,21], as discussed in Method. A low-magnification cross-section image (Fig. 2a) depicts the multilayer stacks of the CTM sample fabricated by focused ion beam (FIB) technology (see Supplementary Fig. S1) and the high-magnification image (Fig. 2c) show the abrupt interfaces between the functional films where the HfO_2 layer is polycrystalline ($P2_1/c$, $a=5.117$ Å, $b=5.175$ Å, $c=5.291$ Å, $\alpha=90°$, $\beta=99.216°$, $\gamma=90°$; polycrystalline morphology is shown in Supplementary Fig. S2). Those HfO_2 grains with different orientation may induce various dynamic diffraction phase as the uneven feature in the phase map of the HfO_2 layer without bias (Fig. 2d). The I–V curve of the pristine sample in the wafer test (Fig. 2b) indicates that current tunnelling or electron injecting erupts above 5 V, whereas the C–V measurement shows a discernible storage winder opened at 8 V (see Supplementary Fig. S3). Considering the background current of the galvanometer, *in situ* electric measurements of the FIB-cutting sample in TEM from a wafer different to 'wafer test' one,

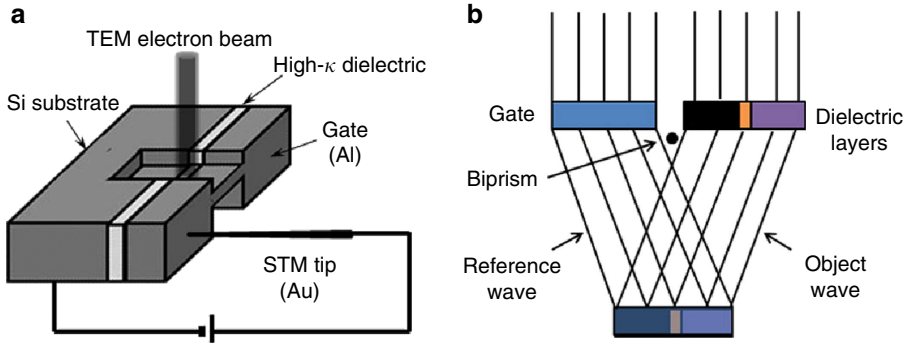

Figure 1 | Schematic diagrams of *in situ* TEM electron holography. (**a**) The set-up of the *in situ* experiment, (**b**) the optical principle of electron holography.

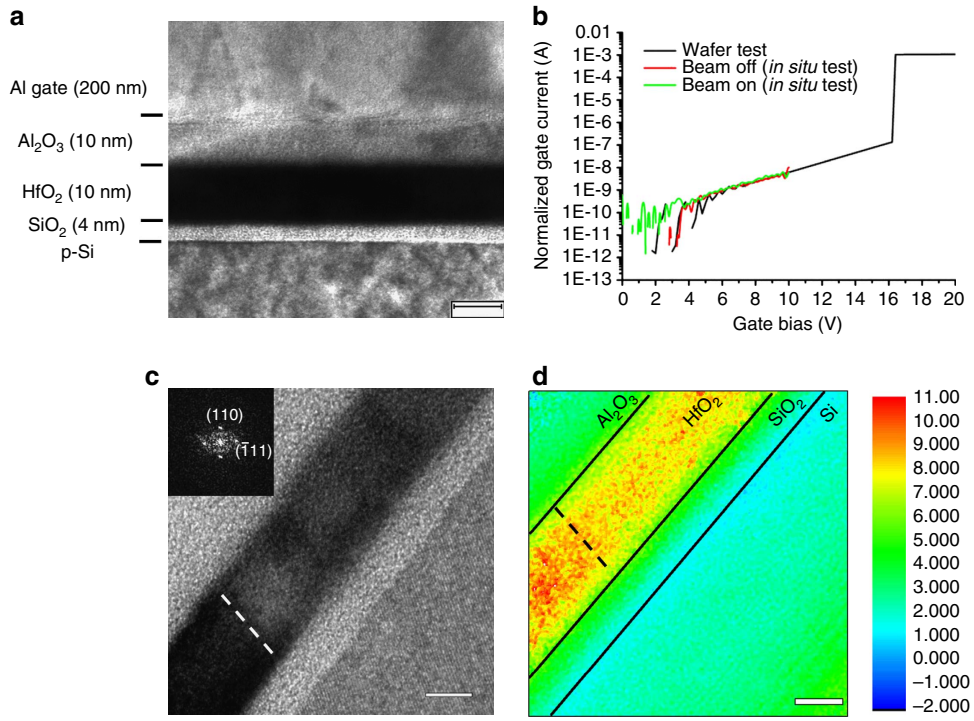

Figure 2 | Structure and I–V behaviour of the CTM sample. (**a**) The low-magnification cross-section image of the CTM sample. (**b**) The normalized I–V curves measured on the wafer and in TEM, with and without electron beam illumination (black: wafer test, red: *in situ* test with beam off, green: *in situ* test with beam on). (**c**) The high-magnification image of the polycrystalline HfO_2 layer, the insert is the fast Fourier transform of one HfO_2 grain. (**d**) The phase image of the unbiased CTM sample involving the three dielectric stacks and the Si substrate; the uneven phase in HfO_2 layer come from the polycrystalline feature. The dashed lines in **c** and **d** indicate the position of grain boundary. Scale bar, 10 nm (**a**), 5 nm (**b**), 5 nm (**c**).

with and without electron beam illuminating, demonstrate the similar charging behaviour and apparently the electron beam shower has the negligible impact on *in situ* test results.

Characterizing the charge location. After stripping off the inner potential and the dynamic diffraction effect, bias-induced phase features $\Delta\varphi^{bias}(x,y)$ of the high-κ dielectric HfO_2 layer together with the whole SiO_2 interlayer, parts of Al_2O_3 block layer and Si substrate readily display the phase evolution in the HfO_2 layer under different bias (Fig. 3). The projected charge density maps $\sigma_{pro}^{bias}(x,y)$calculated from the second differential of $\Delta\varphi^{bias}(x,y)$ images are shown in Fig. 4, with the relative permittivities of 9 for Al_2O_3, 20 for HfO_2, 3.9 for SiO_2 and 11.7 for Si. The projected charge density maps illustrate unambiguously that the charges aggregate unevenly and diffuse laterally within the HfO_2 layer with increasing bias. The negative charge centroid locates near the interface between the HfO_2 film and the Al_2O_3 and lateral migration is also along this interface where a large amount of traps may exist there.

An interesting feature is the positive charges locating near the interface between HfO_2 and SiO_2 films. Usually, the external voltage applied to the dielectric capacitor could cause the negative/positive dipole layer whose positive charges locate near the cathode, whereas the negative charges place beneath the anode, which is out of the observation field. In addition, tunnelling current inducing positive charges (or current-generated positive charges), which have been studied abundantly in the SiO_2 gate insulator of the MOS structures since the early 1980s should be another important source[22,23]. It is speculated indirectly from the electric measurements that the positive charges can be generated and even become the overwhelming trapped charges in the SiO_2 film when tunnelling electrons pass through the gate insulator[22,23]. Similar behaviour was also observed in high-κ stack MOS devices[7,24,25]. To rule out the parasitic dipoles and grasp a semiquantitative estimation of the injected charge distribution, the line phase profiles averaged in the rectangle of each phase map have been fitted with COMSOL Multiphysics simulation software under Gaussian distribution assumption of the injected electrons and current-generated positive charges (see Methods). The fitted curves (Fig. 5) coinciding well with the experimental data supply the quantitative estimation of the charge distribution and the variation with bias change. The charge distribution excluding the dipolar charges as well as the net charges and the effective charge density from the fitted data are plotted in Fig. 6. Although the centroid of the projected charge density in Fig. 4 seems on the top of the HfO_2 film, the simulated results display thoroughly that the centroid should be near the interface between Al_2O_3 block layer and HfO_2 trapping layer. The possibility of negative charge trapping in the middle of HfO_2 or in the interface between HfO_2 and SiO_2 could be excluded here. As expected, the effective charges are negative although the mount of positive charges grows simultaneously. It also explains why those positive charges are seldom recognized in the charge-trapping process characterized with traditional electric measurement, which can only detect the effective or net charges and conceal the existence of positive charges. Now, not only the exact location of the negative charges but also the figure of the positive charges is visualized in the dielectric stacks with high spatial resolution. The inversed layer generated within the *p*-Si substrate also appears as a slight negative stripe beneath the SiO_2 dielectric film. The results also demonstrate that electron holography can detect several hundreds of electrons within a small region.

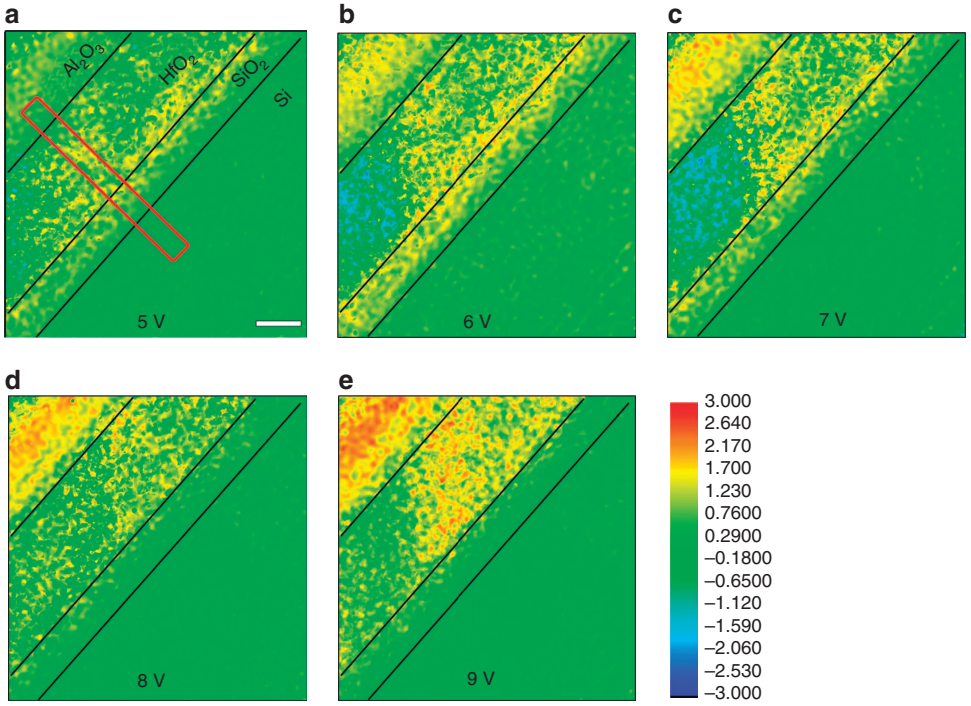

Figure 3 | Bias-induced phase feature $\Delta\varphi^{bias}(x,y)$ under different bias. (**a**) 5 V, (**b**) 6 V, (**c**) 7 V, (**d**) 8 V, (**d**) 9 V. Scale bar, 5 nm.

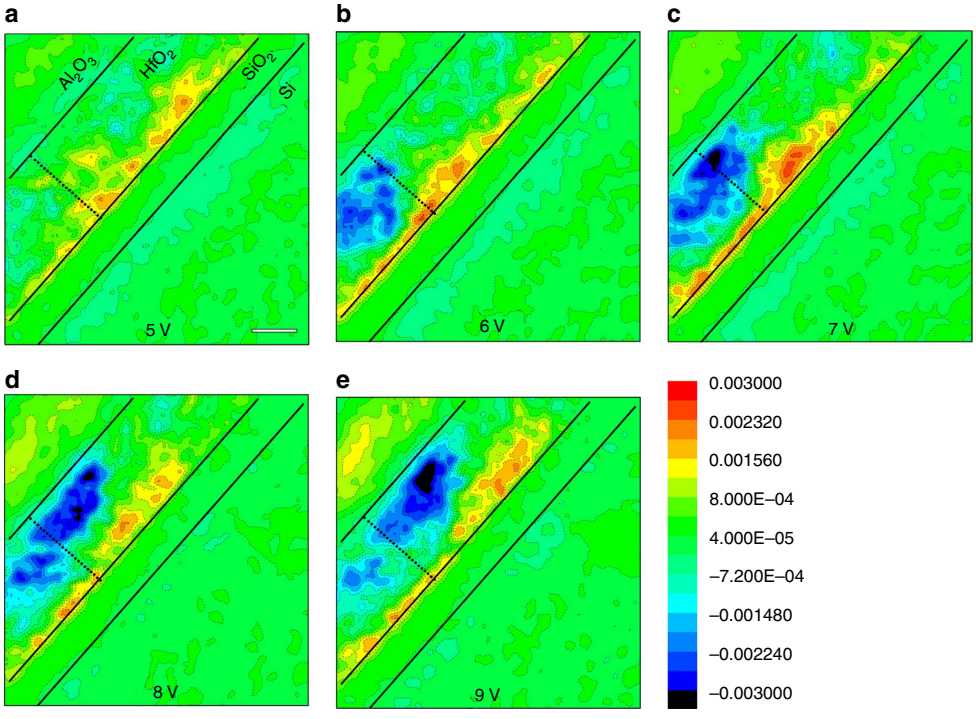

Figure 4 | Projected charge density $\sigma_{pro}^{bias}(x,y)$ maps under different bias. (**a**) 5 V, (**b**) 6 V, (**c**) 7 V, (**d**) 8 V, (**d**) 9 V. The top-left Al_2O_3 layer locates in the Fresnel stripes of the hologram; hence, its second differential result may deviate from the true value in some degree. The inversed layer of *p*-Si can be observed beneath the SiO_2 film as a slight negative stripe. The dashed lines indicate the position of grain boundary, as shown in Fig. 2c,d. Scale bar, 5 nm.

Charging process. Subsequently, the charging scenario can be portrayed based on the above results. Under a lower bias, the Fowler–Nordheim tunnelling mechanism occurs, although the situation is more complicated in HfO_2 stacks than in pure SiO_2 film[26]. The band diagram is shown in Supplementary Fig. S4. The tunnelling electrons move towards the anode and the positive charges generated by trap creation, impact ionization[27], or the defects in the HfO_2 layer[28–32] move oppositely. The hydrogenous species releasing hydrogen in the insulator HfO_2 or SiO_2 may be another source of the positive charges[33]. The possibility of gate-injected holes could be ruled out as the distance between the gate and Si substrate is 24 nm and the injected holes may be

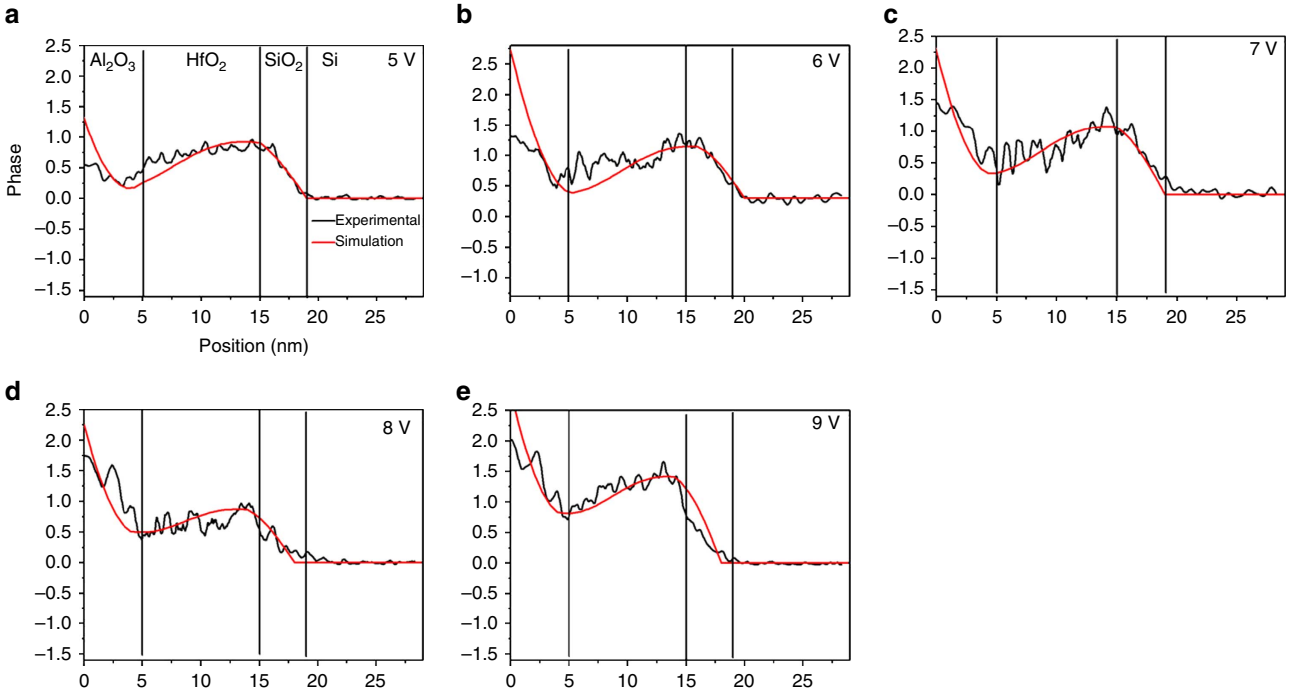

Figure 5 | Experimental and the simulated phase profiles. (**a**) 5 V, (**b**) 6 V, (**c**) 7 V, (**d**) 8 V, (**e**) 9 V. Experimental data are averaged from the rectangles in Fig. 3, plotted with simulated phase curve. The flat phase in the Si region confirms the uniform thickness of the sample.

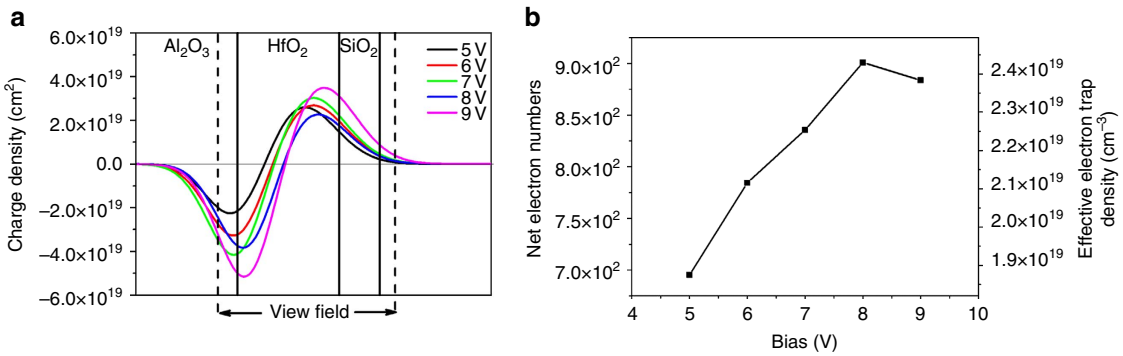

Figure 6 | Negative and positive charge distribution. (**a**) Charge distribution for the simulation and (**b**) corresponding net charges and effective charge density in the whole stacks.

neutralized halfway and cannot aggregate on the observed place. Different from the thin-SiO_2-film MOS transistor where the tunnelling electrons are absorbed immediately by the anode gate, part of the tunnelling electrons would be blocked beneath the Al_2O_3 layer, whereas the positive charges would be trapped a tunnelling distance above the Si surface[27]. Some positive charges will tunnel back to the substrate under the positive gate bias. The reported 5 nm tunnelling distance of those positive charges under low bias press[34] indicates that the residual positive charges should be 5 nm above the silicon substrate, or just 1 nm above the 4 nm SiO_2 interlayer, consistent with the observed positive charge location. With increasing bias, an amount of tunnelling electrons may pour into the HfO_2 layer through some weak points in the SiO_2 film. The degradation spots in the thin SiO_2 film due to local soft breakdown[27] or progressive breakdown[35] by positive charge may be another possible injection point. The electrons would migrate vertically faster along the HfO_2 grain boundary[36–38] because of the higher vertical electric strength so that the electrons aggregate first beneath the Al_2O_3 block layer and later diffuse along the interface between Al_2O_3 and HfO_2, as demonstrated sequentially in Fig. 4. The positive charges trapped near the bottom of HfO_2 cannot be neutralized completely at once, as both injection channel and electron diffusion are spatially limited and inhomogeneous, although the total negative charges surpassing the positive charges result in the net electrons trapping throughout the C–V or I–V characterization. The coexistence of the negative and positive charges cannot be discerned by general electric diagnoses, which feature the effective charge behaviour only as well as SPM with charge force detector whose resolution is too poor to distinguish the vertical charge spatial separation. The positive charge layer neglected in the previous pr ogramming studies with or without modelling analysis should be taken seriously because it may have a contradictory role that not only enhances the electron tunnelling through SiO_2 film to accelerate the charging process[26] but also increases the risk of SiO_2 breakdown and the retention charge loss[39], affecting the programming/erasing performance and the device reliability[40,41]. The uneven

distribution of the positive and negative charges may reflect that the charge traps do not distribute uniformly in the nanoscale because of the grains in the HfO_2 layer, although the local morphology of the interface seems flate.

Influence of illuminating electron beam. The high-energy (200 kV) electrons of the illuminating beam could be trapped or produce holes in the dielectric layers, which may be involved in the charge distribution. However, the number of those electrons or holes should be invariable because of the fixed dose of illumination; hence, it is hard to attribute the change of the charges' amount and location in Figs 3 and 4 to the impact of the high-energy electron beam. The charges' evolution and their location in the sample studied here may be also influenced by the surface depletion in the thin TEM sample as well as the unavoidable FIB-cutting damage, which possibly induces SiO_2 degradation or causes the larger current leakage, deviating from the pristine materials. Considering the physical or chemical sculpturing process during devices fabrication and the tiny size of the next-generation memory unit, the charge-trapping behaviour revealed with the *in situ* electron holography here still shows the significance to the future actual memory devices. The phase images acquired under different illumination dose also confirm that the intensity of the electron shinning beam can be neglected compared with the bias effect (see Supplementary Fig. S5).

Recombination without bias. Another noteworthy point is that the bias is no more than 9 V in this paper because of the voltage ceiling of the *in situ* voltmeter. If the bias press increases higher, the injected electrons should fill more part of the interface between HfO_2 and SiO_2. However, whether the positive charges are annihilated completely is yet to be confirmed in future. Further, not the charge retention location but the charging process is monitored here. If the bias disappears, the negative and positive charges could recombine to result in a redistribution of charges[42], and it may be in a steady-state manner different from the observation here.

Discussion

Charge-pumping method[43] is more sensitive to the surface state, so it is employed to find the charges trapped on or close to the interface between SiO_2 and the trap layer[44,45], but it is difficult to detect the negative charges locating deeply in the HfO_2 layer. Transient analysis method can demonstrate the centroid of the charges not only on the interfaces but also inside the trap layer[46,47]. However, it could not display the spatial details about the charges' distribution and relationship between such distribution and the device morphology. Here *in situ* electron holography visualizes the detailed scenery of the local charge distribution and its evolution in the high-κ charge-trapping devices under varied bias for the first time. The extracted phase changes induced by bias stress with high spatial resolution reveal the coexistence of the negative and positive charges during charging process, which was neglected by the previous electric characterization and theory analysis. The electrons injected under higher bias may pass through the HfO_2 grain boundary and accumulate near the interface between Al_2O_3 and HfO_2 dielectric layers, whereas the positive charges are trapped in the interface between the HfO_2 and SiO_2 films. The discovered positive charges that have been studied in the SiO_2 gate insulator for many years are seldom considered in electron tunnelling of high-κ CTM structures before but should arise enough attention as the positive charges may influence the device performance, especially the lifetime as well as the impact on the breakdown of the anodic SiO_2 in MOS structures. The species of the positive charges and the relationship between the inhomogeneous electron injection and the uneven structure features of HfO_2 film should be clarified by the on-going work. The trapping level of the charges revealed that the *in situ* electron holography should also be analysed combined with other methods, including theory calculation, in future works. The studied HfO_2 trapping structures are something different with the silicon–oxide–nitride–oxide–silicon systems; thus, the charge distribution uncovered here may be not as same as in the silicon–oxide–nitride–oxide–silicon devices.

Methods

High-κ charge memory sample. The HfO_2-based CTM sample was prepared as follows. The *p*-type Si (100) wafers with a resistivity of 8–12 Ω were cleaned by the standard Radio Corporation of America process. Then, a 4-nm SiO_2 film acting as the tunnelling layer was thermally grown in dry O_2 ambience. Two layers of Al_2O_3 and HfO_2 with thicknesses of 10 nm were deposited sequentially on the SiO_2 film. All the films were deposited *in situ* by atomic layer deposition at a substrate temperature of 250 °C. Post-deposition annealing process was carried out in N_2 ambience under 700 °C for 1 min. Finally, a 200-nm thick Al gate electrode was formed by a lift-off process.

***In situ* holography characterization.** The CTM samples were mechanically milled and then cut by FIB with ±2° refinement to guarantee the uniform thickness. Additional 5 s ion milling was performed to remove the surface amorphous layers and the possible dead layers. The thickness of the sample for holography study was about 150 nm, characterized with electron energy loss spectroscopy (see Supplementary Fig. S6), which agrees well with the measurement in SEM image (see Supplementary Fig. S1c). The sample was installed on a Nanofactory *in situ* holder, which can manipulate the Au tip to apply the voltage to the Al gate of the sample and monitor the current at the same time. Electron holograms were recorded in charge-coupled device camera of Tecnai F20 electron microscope equipped with holography biprism. Standard vacuum reference hologram was pictured first to correct the phase distortion from the optical system while the *in situ* electron holograms were recorded with the reference wave penetrating the Al gate because the limited view field of hologram at high magnification cannot place the vacuum region over the interesting high-κ layers buried deeply below the Al gate.

The reference hologram (Supplementary Fig. S7a) is used to estimate the spatial resolution. The sideband location in the fast Fourier transform of the reference hologram (Supplementary Fig. S7b) corresponds to a 0.22-nm resolution ($\vec{\mathbf{q}}_c = 4.61/nm$). Not $\vec{\mathbf{q}}_c/3$ in the most cases but $\vec{\mathbf{q}}_c/5$ is employed to reconstruct the phase image to improve the signal-to-noise ratio, and thus the retrieved spatial resolution is down to about 1 nm, which is enough for the investigation. The holography reconstruction is completed with the plug-in HoloWork in Digital Micrography of Gatan, and the unwrapping processing is achieved with a published code[48]. The contrast of the interference fringes in the sample hologram is also degraded from 8 to 3.5% because of the deterioration of the beam coherence. Therefore, many extracted phase images are averaged to obtain the enough phase resolution (Supplementary Fig. S7c,d).

For a sample, the image processing to extract the bias-induced phase map $\Delta\varphi^{5V}(x,y)$ is shown here. $\Delta\varphi^{5V}(x,y)$ (Fig. 3a) is calculated by Supplementary Fig. S8 subtracting Supplementary Fig. 2d directly after the image alignment. As discussed below, using electron beam from Al gate as reference wave will not confuse the analysis of charge-induced phase modulation in the high-κ dielectric film. It also avoids the risk of stray field disturbance in the conventional scheme where the phase of the vacuum reference wave could be distorted by the stray field of gate or electrode[49] but the phase resolution is sacrificed because of the coherence deterioration of the penetrating wave[50]. Thus, at least 20 retrieved phase images for each bias were averaged to obtain the final phase distribution, including 0 V image, which was subtracted as the 'background' from the phase maps under bias. The statistical s.d. 0.1 in the Si substrate in Fig. 3a could be an estimation of the phase resolution here because the bias-induced phase in the grounded Si substrate should be a constant. The sample drift was corrected by post-alignment of holograms with the mark in the sample. Thus, the resulted image size was only 805 × 823 pixels although the original image size was 1,024 × 1,024 pixels. The gate bias was kept during the acquirement of the hologram.

The phase distribution of the reconstructed image including the dielectric stacks and Si substrate without gate bias $\varphi^{0V}(x,y)$ is determined by the phase difference between the objective phase containing $\varphi^{\mathrm{iner}}_{\mathrm{obj}}(x)$ and $\varphi^{\mathrm{dyn}}_{\mathrm{obj}}(x,y)$ and the reference gate phase involving $\varphi^{\mathrm{iner}}_{\mathrm{gate}}(x,y)$ and $\varphi^{\mathrm{dyn}}_{\mathrm{gate}}(x,y)$, where 'iner' and 'dyn' indicate the mean inner potential and the possible dynamic diffraction effect, respectively.

$$\varphi^{0V}(x,y) = \varphi^{\mathrm{iner}}_{\mathrm{obj}}(x,y) + \varphi^{\mathrm{dyn}}_{\mathrm{obj}}(x,y) - \varphi^{\mathrm{iner}}_{\mathrm{gate}}(x,y) - \varphi^{\mathrm{dyn}}_{\mathrm{gate}}(x,y) \quad (1)$$

It is apparent that $\varphi^{\mathrm{iner}}_{\mathrm{obj}}(x)$, $\varphi^{\mathrm{dyn}}_{\mathrm{obj}}(x,y)$, $\varphi^{\mathrm{iner}}_{\mathrm{gate}}(x,y)$ and $\varphi^{\mathrm{dyn}}_{\mathrm{gate}}(x,y)$ are the intrinsic physical property of the sample and the orientation correlated effect, which do not vary under bias. When a bias is applied to the gate, the phase $\varphi^{\mathrm{bias}}(x,y)$ should be

changed to

$$\varphi^{\mathrm{bias}}(x,y)=\varphi^{\mathrm{iner}}_{\mathrm{obj}}(x,y)+\varphi^{\mathrm{dyn}}_{\mathrm{obj}}(x,y)+\varphi^{\mathrm{bias}}_{\mathrm{obj}}(x,y)-\varphi^{\mathrm{iner}}_{\mathrm{gate}}(x,y)-\varphi^{\mathrm{dyn}}_{\mathrm{gate}}(x,y)-\varphi^{\mathrm{bias}}_{\mathrm{gate}}(x,y) \quad (2)$$

where $\varphi^{\mathrm{bias}}_{\mathrm{obj}}(x,y)$ is the phase shift caused by the trapped charges and $\varphi^{\mathrm{bias}}_{\mathrm{gate}}(x,y)$ is the additional phase by the bias. Thus, the reconstructed $\varphi^{\mathrm{bias}}(x,y)$ contains not only the features induced by the gate bias but also the contributions of the mean inner potential and the dynamic diffraction similar to $\varphi^{0V}(x,y)$. After a careful image alignment, $\varphi^{0V}(x,y)$ could be subtracted from $\varphi^{\mathrm{bias}}(x,y)$ and then the bias-induced phase feature $\Delta\varphi^{\mathrm{bias}}(x,y)$ should be,

$$\Delta\varphi^{\mathrm{bias}}(x,y)=\varphi^{\mathrm{bias}}(x,y)-\varphi^{0V}(x,y)=\varphi^{\mathrm{bias}}_{\mathrm{obj}}(x,y)-\varphi^{\mathrm{bias}}_{\mathrm{gate}}(x,y). \quad (3)$$

It is reasonable to assume that the bias-caused phase shift $\varphi^{\mathrm{bias}}_{\mathrm{gate}}(x,y)$ should be a constant or acts as a uniform phase background $\varphi^{\mathrm{bias}}_{\mathrm{gate}}$ because the metal gate could be regarded as an equipotential under given bias. Therefore, $\Delta\varphi^{\mathrm{bias}}(x,y)$ could be presented as

$$\Delta\varphi^{\mathrm{bias}}(x,y)=\varphi^{\mathrm{bias}}_{\mathrm{Si}}(x,y)+\varphi^{\mathrm{bias}}_{\mathrm{diele}}(x,y)-\varphi^{\mathrm{bias}}_{\mathrm{gate}} \quad (4)$$

where $\varphi^{\mathrm{bias}}_{\mathrm{obj}}(x,y)$ is substituted by $\varphi^{\mathrm{bias}}_{\mathrm{Si}}(x,y)$ and $\varphi^{\mathrm{bias}}_{\mathrm{diele}}(x,y)$, indicating the phase shift of Si substrate and the dielectric layers in the view field, respectively. The attention is focused on the phase shift of the insulator stacks because $\varphi^{\mathrm{bias}}_{\mathrm{Si}}(x,y)$ may also be an invariant feature $\varphi^{\mathrm{bias}}_{\mathrm{Si}}$ because of the grounded Si substrate, confirmed by the flat phase configuration of Si in Figs 3 and 5. Further, the expression of $\Delta\varphi^{\mathrm{bias}}(x,y)$ is very simple now:

$$\begin{aligned}\Delta\varphi^{\mathrm{bias}}(x,y)&=\varphi^{\mathrm{bias}}_{\mathrm{Si}}+\varphi^{\mathrm{bias}}_{\mathrm{diele}}(x,y)-\varphi^{\mathrm{bias}}_{\mathrm{gate}}\\&=\varphi^{\mathrm{bias}}_{\mathrm{Si}}+C_{\mathrm{E}}V_{\mathrm{pro}\,\mathrm{diele}}^{\mathrm{bias}}(x,y)t-\varphi^{\mathrm{bias}}_{\mathrm{gate}}\end{aligned} \quad (5)$$

where C_{E} is 0.0073/(V nm) for 200 kV electrons, $V_{\mathrm{pro}\,\mathrm{diele}}^{\mathrm{bias}}(x,y)$ is the 'projected' (along electron beam direction z) potential induced by bias in dielectric layers and t is the sample thickness measured with EELS, 150 nm. Thus, the charge distribution would also result in a strong phase change predominantly in the insulator films, as shown in Fig. 3. According to the Poisson equation, the projected charge density $\sigma^{\mathrm{bias}}_{\mathrm{pro}}(x,y)$in the dielectric layer is[51]

$$\begin{aligned}\sigma^{\mathrm{bias}}_{\mathrm{pro}}(x,y)&=-\epsilon\nabla^2V_{\mathrm{pro}\,\mathrm{diele}}^{\mathrm{bias}}(x,y)=-\frac{\epsilon\nabla^2[\varphi^{\mathrm{bias}}_{\mathrm{diele}}(x,y)]}{C_{\mathrm{E}}t}\\&=-\frac{\epsilon\nabla^2[\Delta\varphi^{\mathrm{bias}}(x,y)]}{C_{\mathrm{E}}t}\end{aligned} \quad (6)$$

where ϵ is the dielectric constant. Therefore, the lateral- and vertical-projected charge density distribution could be extracted directly from the second differential of $\Delta\varphi^{\mathrm{bias}}(x,y)$ map.

Simulation. The multilayer model for simulation is shown in Supplementary Fig. S9. The Gaussian distribution is assumed both for negative and positive charges in the HfO_2 layer. The relative permittivities are 9 for Al_2O_3, 20 for HfO_2, 3.9 for SiO_2 and 11.7 for Si. For the lack of the information from the negative charges due to the polarization, the invariable negative charge density $5\times10^{19}\,\mathrm{cm}^{-3}$ has been assumed in the Al_2O_3 block layer for the convenience.

References

1. You, H. –W. & Cho, W. –J. Charge trapping properties of the HfO_2 layer with various thickness for charge trap flash memory application. *Appl. Phys. Lett.* **96,** 093506 (2010).
2. Zhu, C. *et al.* Performance enhancement of multilevel cell nonvolatile memory by using a bandgap engineered high-κ trapping layer. *Appl. Phys. Lett.* **97,** 253503 (2010).
3. Bu, J. & White, M. H. Design considerations in scale SONOS nonvolatile memory devices. *Solid-State Electron* **45,** 113–120 (2001).
4. Zahid, M. B., Arreghini, A., Degraeve, R. & Govoreanu, B. Electron trap profiling near Al_2O_3/gate interface in TANOS stack using gate-side trap spectroscopy by charge injection and sensing. *IEEE Electr. Dev. Lett.* **31,** 1158–1160 (2010).
5. Rao, R., Lorenzi, P., Ghidini, G., Palma, F. & Irrera, F. Eletron-related phenomena at the TaN/ Al_2O_3 interface. *IEEE Trans. Electr. Dev.* **57,** 637–643 (2010).
6. Padovani, A. *et al.* Charge trapping in alumina and its impact on the operation of metal-alumina-nitride-oxide-silicon memories: Experiments and simulations. *J. Appl. Phys.* **110,** 014505 (2011).
7. Sharama, S. K., Prasad, B. & Kumar, D. Application of high-κ dielectric stacks charge trapping for CMOS technology. *Mater. Sci. Eng. B* **166,** 170–173 (2010).
8. Ko, C., Shandalov, M., Mclntyre, P. & Ramanathan, S. High temperature electrical conduction in nanoscale hafnia films under varying oxygen partial pressure. *Appl. Phys. Lett.* **97**(082102): 1–3 (2010).
9. Ramanathan, S., Mclntyre, P. C., Guha, S. & Gusev, E. Charge trapping studies on ultrathin ZrO_2 and HfO_2 high-κ dielectrics grown by room temperature ultraviolet ozone oxidation. *Appl. Phys. Lett.* **84,** 389–391 (2004).
10. Baik, S. J. & Lim, K. S. Charge diffusion in silicon nitrides: scalability assessment of nitride based flash memory. *IRPS 6B* **4,** 1 (2011).
11. Lwin, Z. Z. *et al.* Localized charge trapping and lateral charge diffusion in metal nanocrystal-embedded high-κ/SiO_2 gate stack. *Appl. Phys. Lett.* **99,** 222102 (2011).
12. Lin, Z., Bremond, G. & Bassani, F. Memory properties and charge effect study in Si nancrystals by scanning capacitance microscopy and spectroscopy. *Nanoscale Res. Lett.* **6,** 163 (2011).
13. Fiorenza, P., Polspoel, W. & Vandervorst, W. Conductive atomic force microscopy studies of thin SiO_2 layer degradation. *Appl. Phys. Lett.* **88,** 222104 (2006).
14. Rau, W. D., Schwander, P., Baumann, F. H., Höppner, W. & Ourmazd, A. Two-dimensional mapping of the electrostatic potential in transistors by electron holography. *Phys. Rev. Lett.* **82,** 2614–2617 (1999).
15. Deguchi, M., Tanaka, S. & Tanji, T. Determination of piezoelectric fields across InGaN/GaN quantum wells by means of electron holography. *J. Electron. Mater.* **39,** 815–818 (2010).
16. Wei, Q. Y., Wu, Z. H., Ponce, F. A., Hertkorn, J. & Scholz, F. Polarization effects in 2-DEG and 2-DHG AlGaN/AlN/GaN multi-heterostructures measured by electron holography. *Phys. Status Solidi B* **247,** 1722–1724 (2010).
17. Li, L. *et al.* Polarization-induced charge distribution at homogeneous zincblende/wurtzite heterostructural junctions in ZnSe nanobelts. *Adv. Mater.* **24,** 1328–1332 (2012).
18. Twitchett, A. C., Dunin-Borkowski, R. E. & Midgley, P. A. Quantitative electron holography of biased semiconductor devices. *Phys. Rev. Lett.* **88,** 238302 (2002).
19. Ikarashi, N., Takeda, H., Yako, K. & Hane, M. *In-situ* electron holography of surface potential response to gate voltage application in a sub-30-nm gate-length metal-oxide-semiconductor field-effect transistor. *Appl. Phys. Lett.* **100,** 143508 (2012).
20. Yao, Y. *et al.* Electron holography characterization of the electrostatic potential of thin high-κ dielectric film embedded in gate stack. *Appl. Phys. Lett.* **99,** 163506 (2011).
21. Hÿtch, M., Houdellier, F., Hüe, F. & Snoeck, E. Nanoscale holographic interferometry for strain measurements in electronic devices. *Nature* **453,** 1086–1089 (2008).
22. Jeno, C. S., Ranganath, T. R., Huang, C. H., Jones, H. S. & Chang, T. T. L. High-field generation of electron traps and charge trapping in ultra-thin SiO_2. *IEDM* **27,** 388–391 (1981).
23. Liang, M. –S., Chang, C., Tong, Y., Hu, C. M. & Brodersen, R. W. MOSFET degradation due to stressing of thin oxide. *IEEE Trans. Electr. Dev.* **31,** 1238–1244 (1984).
24. Zhao, C. Z., Zhang, J. F. & Zahid, M. B. Impact of gate materials on positive charge formation in HfO_2/SiO_2 stacks. *Appl. Phys. Lett.* **89,** 023507 (2006).
25. Zhao, C. Z. *et al.* Stress-induced positive charge in Hf-based gate dielectrics: impact on device performance and a framework for the defect. *IEEE Trans. Electr. Dev.* **55,** 1647–1656 (2008).
26. Paskaleva, A., Lemberger, M., Atanassova, E. & Bauer, A. J. Traps and trapping phenomena and their implications on electrical behavior of high-κ capacitor stacks. *J. Vac. Sci. Tech. B* **29,** 01AA03–01AA10 (2011).
27. Dimaria, D. J., Cartier, E. & Arnold, D. Impact ionization, trap creation, degradation, and breakdown in silicon dioxide films on silicon. *J. Appl. Phys.* **73,** 3367–3384 (1993).
28. Xiong, K. & Robertson, J. Point defects in HfO2 high-κ gate oxide. *Microelectron. Eng.* **80,** 408–411 (2005).
29. Onishi, K. *et al.* Bias-temperature instabilities of polysilicon gate HfO_2 MOSFETs. *IEEE Trans. Electr. Dev.* **50,** 1517–1524 (2003).
30. Houssa, M. *et al.* Electrical properties of high-κ gate dielectrics: challenges, current issues, and possible solutions. *Mater. Sci. Eng. R* **51,** 37–85 (2006).
31. Zafar, S., Kumar, A., Gusev, E. & Cartier, E. Threshold voltage instabilities in high-κ gate dielectric stacks. *IEEE Trans. Dev. Mater. Reliab.* **5,** 45–64 (2005).
32. Xiong, K., Du, Y., Tse, K. & Robertson, J. Defect states in the high-dielectric-constant gate oxide $HfSiO_4$. *J. Appl. Phys.* **101**(024101): 1–7 (2007).
33. Suñé, J. & Wu, E. Y. Hydrogen-release mechanisms in the breakdown of thin SiO_2 films. *Phys. Rev. Lett.* **92,** 087601 (2004).
34. DiMaria, D. J., Weinberg, Z. A. & Aitken, J. M. Location of positive charges in SiO_2 films on Si generated by VUV photons, X rays, and high-field stressing. *J. Appl. Phys.* **48,** 898–906 (1977).
35. Lombardo, S. *et al.* Dielectric breakdown mechanism in gate oxides. *J. Appl. Phys.* **98,** 121301 (2005).
36. Lwin, Z. Z., Pey, K. L. & Chen, Y. N. Charging and discharging characteristic of metal nanocrystals in degraded dielectric stacks. *IPRS 2C* **3,** 1 (2010).
37. Kim, B. *et al.* Investigation of ultra thin polycrystalline silicon channel for vertical NAND flash. *IPRS 2E* **4,** 1 (2011).
38. Yao, J., Zhong, L., Natelson, D. & Tour, J. M. *In situ* imaging of the conducting filament in a silicon oxide resistive switch. *Sci. Rep.* **2,** 242 (2012).
39. Vogel, E. M., Heh, D. -W., Bernstein, J. B. & Suehle, J. S. Impact of the trapping of anode hot holes on silicon dioxide breakdown. *IEEE Electr. Dev. Lett.* **23,** 667–669 (2002).

40. Vandelli, L., Padovani, A. & Larcher, L. Role of holes and electrons during erase of TANOS memories: evidences for dipole formation and its impact on reliability. *IRPS* **737** (2010).
41. Ribes, G. *et al.* Review of high-κ dielectric reliability issues. *IEEE Trans. Dev. Mater. Reliab.* **5,** 5–19 (2005).
42. Mang, K. M. *et al.* Direct imaging of charge redistribution in a thin SiO_2 layer. *Europhys. Lett.* **67,** 261–266 (2004).
43. Groeseneken, G., Maes, H. E., Beltran, N. & De Keersmaecker, R. F. A reliable approach to charge-pumping measurement in MOS transistors. *IEEE Trans. Electr. Dev.* **31,** 42–53 (1984).
44. Chen, C. & Ma, T. –P. Direct lateral profiling of hot-carrier-induced oxide charge and interface traps in thin gate MOSFET's. *IEEE Trans. Electr. Dev.* **45,** 514–520 (1998).
45. An, H. –M. *et al.* A direct observation of the distributions of local trapped-charges and the interface-states near the drain region of the silicon-oxide-nitride-oxide-silicon device for reliable four-bit/cell operations. *Jpn J. Appl. Phys.* **49,** 114203 (2010).
46. Lue, H. –T. *et al.* A study of gate-sensing and channel-sensing (GSCS) transient analysis method—part I: fundamental theory and applications to study of the trapped charge vertical location and capture efficiency of SONOS-type devices. *IEEE Trans. Electr. Dev.* **55,** 2218–2228 (1998).
47. Seo, Y. J. *et al.* Investigation of vertically trapped charge locations in Cr-doped-$SrTiO_3$-based charge trapping memory devices. *J. Appl. Phys.* **112,** 074505 (2012).
48. Ghiglia, D. C. & Pritt, M. D. *Two-Dimentional Phase Unwrapping: Theory, Algorithms, and Software* (John Wiley & Sons, Inc., 1998).
49. Lichte, H. & Lehmann, M. Electron holography—basics and applications. *Rep. Prog. Phys.* **71,** 016102 (2008).
50. Smith, D. J. & McCartney, M. R. in *Practical Electron Holography*. (eds Völkl, E., Allard, L. F. & Joy, D. C. Ch. 4 (Kluwer Academic/Plenum Publisher, 1999).
51. McCartney, M. R. *et al.* Quantitative phase imaging of nanoscale electrostatic and magnetic fields using off-axis electron holography. *Ultramicroscopy* **110,** 375–382 (2010).

Acknowledgements

This work was supported by the State Key Development Program for Basic Research of China (Grant numbers 2010CB934202, 2012CB932302 and 2013CB932904), the National Natural Science Foundation of China (Grant number 10974235 and 11274365).

Author contributions

Y.Y. designed the experiments and performed the image processing, data analysis and simulation. C.L. carried out the FIB sample fabrication and hologram acquirement. C.X.Z. fabricated the CTM sample and Z.L.H. participates the experiment design. Y.Y. and R.C.Y. wrote the paper. Y.G.W., X.F.D., L.G., C.Z.G, Z.L.H. and M.L. revised the manuscript. All authors discussed the results and commented on the manuscript.

Additional information

Supplementary Information accompanies this paper at http://www.nature.com/naturecommunications

Competing financial interests: The authors declare no competing financial interests.

Reprints and permission information is available online at http://npg.nature.com/reprintsandpermissions/

How to cite this article: Yao, Y. *et al. In situ* electron holography study of charge distribution in high-κ charge trap memory. *Nat. Commun.* 4:2764 doi: 10.1038/ncomms3764 (2013).